CONTROL OF THE MAIN RING MAGNET POWER SUPPLY FOR THE 12 GeV PS

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ABSTRACT

A new analog and digital hybrid control system has been constructed and optimized for the main ring magnet power supply. In the system, real-time thyristor controls have been carried out by analog voltage and current patterns fed from the digital system through 16-bit DAC by analog control loop of current and of voltage as the negative feed back. The control clock is 600 Hz synchronized ac line voltage.

After reduction of common mode noise, the system with current loop gain 100 works stable and the current ripples have been reduced to a half level or less. Current ripple of QF estimated at 0.07% on injection and 0.008% on flat top.

INTRODUCTION

The hybrid control scheme of analog and digital system for main ring magnet power supply (MPS) of the 12 GeV proton synchrotron has been converted to the new control scheme of the improved analog system and the new multi-microprocessor system H-V90 and twin H-04M, since the first run of this year for a routine operation. General survey of the scheme has been described somewhere(1). The H-V90 and H-04M system engages in fast feedforward pattern control with 600 Hz control clock and in slow but reliable and high gain feedback control for steady deviations to current pattern as periodic control method of current(1,2). The analog system works on the real time feed back control to the voltage and current pattern fed by the digital system.

We report on the improved analog system and interface to digital input and output process controller system of twin H-04M in the multi-cpu. By the hybrid system design(3), two improvements have been carried out on the control scheme. The one is for automatic current regulator (ACR) to be converted from the digital with the 100 Hz control clock to analog with 600 Hz clock. The analog ACR reduce not only the load of the cpu system, but also makes the loop gain up to several or more times the one of digital ACR by small effective dead time. The other is for a minor automatic voltage regulator (MAVR) to make short the dead time to about 1.67 ms, a half of thyristor switching interval of six pulsed bridge, by summing up two bridge voltages of the same pattern group.

ANALOG CONTROL SYSTEM

Fig. 1 gives a schematic block diagrams of the hybrid control system. The analog system covers ACR and MAVR loop as real-time negative feed back (NFB) control to thyristor switching. An ACR is a comparatively slow response, but rather high gain NFB-loop on between the current pattern fed by DAC and the output of DCCT. On the other hand, a MAVR is fast but low gain NFB-loop on between the reference voltage pattern fed by the DAC and the output voltage of the 12 pulsed thyristor bridge group. By a control voltage, an automatic pulse phase shifter (APPS) generates ignition pulses for thyristors of each bridge. The control voltage is sum of pattern signal and MAVR- and ACR-error signal. By 16-bit DAC, the pattern voltages and current are given for every 12-pulsed thyristor groups at 600 Hz control clock synchronized to of ac-line voltage. The analog and dc power parts of the schematic diagram are corresponded respectively to bending-MPS (BPS), horizontally focusing-MPS (QFPS) and defocusing-MPS (QDPS) except number of MAVR loops, which are equal to the number of three phase bridges.

Interface

BPS is controlled by six voltage patterns for 12 pulsed thyristor converter groups and by the current pattern for the ACR. These seven patterns plus two patterns of total reference voltage to thyristor groups and to the B magnet are fed through nine 16-bit DAC sets by the output controller H-04M.

QFPS and QDPS works by a reference voltage to the thyristor group and to the Q magnet and by the current pattern respectively. These three patterns of each MPS are fed through six 16-bit DAC sets by the same output controller.

These fifteen patterns are calculated and distributed on the main system together with bypass timing pattern and with timing pattern from P1 to P5. These timing patterns are output through isolated 16-bit parallel I/O unit as same as those of DAC and ADC.

On the other hand, input controller as the detector system H-04M logs, through three sets of 16-bit ADC, B-, Qf- and Qd-magnet current from DCCT and, through four sets of 16-bit ADC, voltages of two groups of B magnet, Vbl and Vbr, and Qf-, Vqf, and Qd-magnet voltage, Vqd, at the every control clock.

These 15 sets of DAC and seven sets of ADC have been developed by ourselves to fit sever rejection to common noise and to hold exact synchronization.

Common Mode Noise

Though analog ACR reduced the overhead of the cpu system, there were derived troublesome noise problems to be effective directly to a precision of the analog control. The most of all signal inputs were non-equilibrium on the main parts of the analog, except ADC system of the previous main computer system H-350 with 10ms control clock. In spite of these bad circumstances on noises, the old hybrid system had worked reliably, because of single ended input-output system separated to common mode noises by digital ACR.

However, the improved system construction has been added new extended apparatus to the old. Where the apparatus are analog instruments on ACR and MAVR, and are interfacing instruments of ADC and DAC with 600 Hz clock. Therefore, on the most of all paths of pattern and feedback signal, these input and output among the old and the new apparatus are separated by equilibrium input of differential amplifiers to reduce common mode (CMM) noises.

Further, many trials have been executed to reduce the CMM noise for optimization. One of these trials is that three common lines between DCCT and ADC are open.

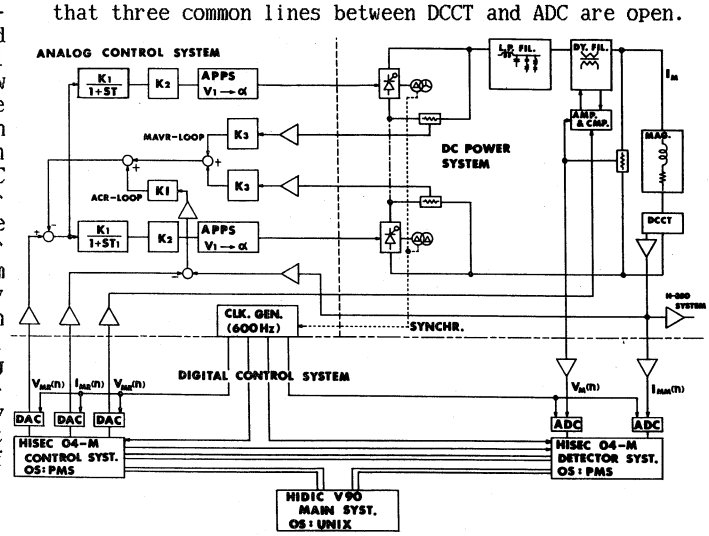
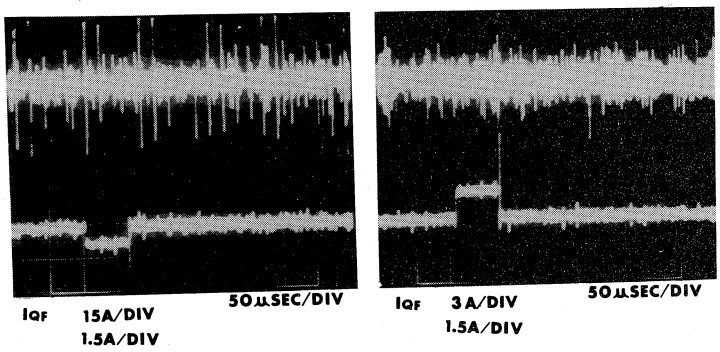


Fig. 1 Schematic whole hybrid control system.



(a) closed common line (b) open common line
Fig. 2 Multi-microprocessor system.

upper: output for ACR, buttered SHA input side
bottom: ouptut for ADC, SHA output side
Olutput point of a measured current signal for the ACR to change from output side to input of sample hold amp (SHA) on the ADC board, because high impedance state, except sampling interval is not preferable in noise level on the input of the ADC. Fig. 2 shows one of these examples for the optimization for CMM noise by output point of ACR. There were similar situations of closed-looping on the common lines of MAVRs and of the buffered output of DCCT for the H-350. These loopings among MAVR paths have been separated by differential amplifiers. The buffered DCCT signals have been separated from the common line of the main output for ADC of H-04M by different control power supply to exclude the closed common line, because the system works parallel on a routine operation of the V-90 system as the tracking monitor by 10 ms sampling clock.

After all, in Fig.1, these differential amplifiers are indicated schematically by symbols of operational amplifier.

RESULTS

After these improvements on analog ACR, the loop gains have been set several times larger than those of the digital ACR on BPS, QFPS and QDPS. In Fig. 3, convergence of ACR deviation of IB by the periodic control of current are given from the initial pattern of 12 GeV to the corrected by eight times after. It seems for the loop gain, 100, to be still increased stable, because any oscillation could not find out at neighborhood of P1 and P3. However, the gain of the digital ACR with 100 Hz clock was about 30 even at maximum. Fig. 4 shows the deviation corrected by 20 times or more after. On the injection, distributed points makes four or six dotted straight lines derived by the current ripple. These spacings between nearest neighbor two lines are correspond to bit resolution of 16 bit-ADC, 45 mA, calibrated the DCCT output 10 V at

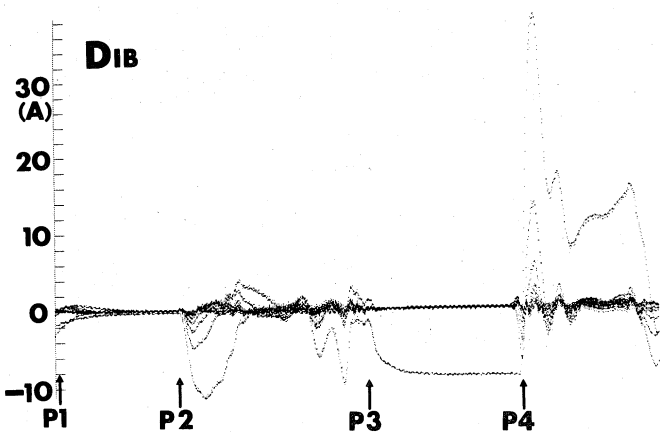


Fig. 3 Typical converging process of measured B-magnet current deviations from the pattern by periodic control method.

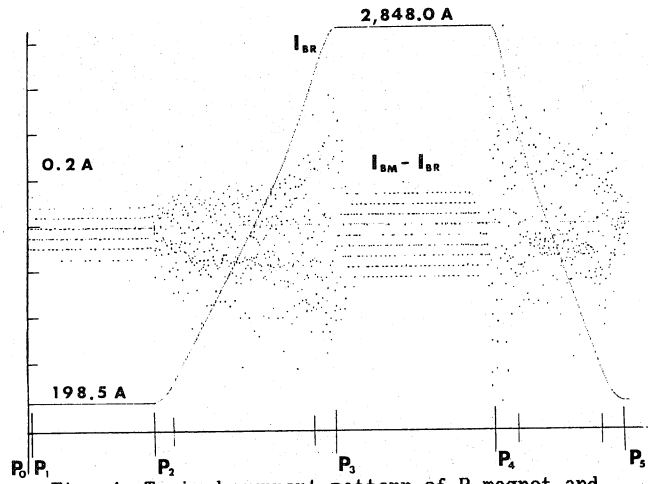


Fig. 4 Typical current pattern of B-magnet and measured current deviation.

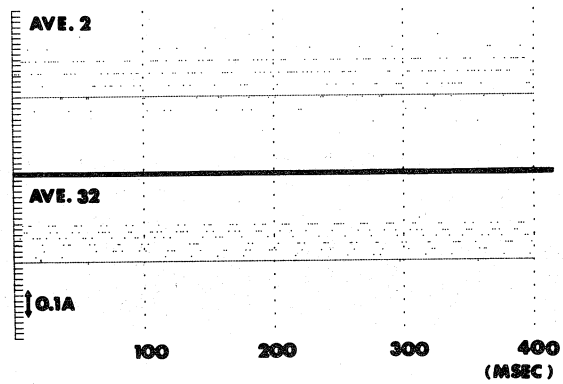
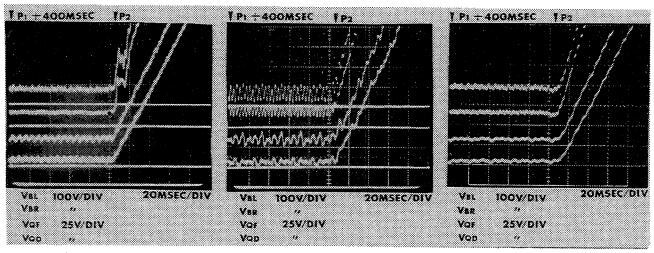


Fig. 5 Sampled current deviation of B-magnet on an injeciton.

3000 A. These data were average values of 16 times sampling. Fig. 5 gives the deviations of twice times and of 32 times averaging at upper and bottom part, respectively. These results suggest for the averaging times to be not important to random errors, but steady errors. These steady errors would be contributed by the intrinsic ripples from modulation frequency of dc currents on the DCCT. There are similar situations on the QFPS and the QDPS.

Fig. 6 gives measured magnet voltages at injection and acceleration start timing on a routine 12 GeV operation. (a) means those voltages controlled by H-350 system. (b) means those by V 90 system with equilibrium input of DAC patterns. (c) means those by present V90 system. Fig. 7 indicates the same voltages at acceleration end and flat top timing, under the same conditions with Fig. 6. In these both figures, VQF and VQD are different from with tracking offsets in (c) and without the offsets in (b.) Those on (c) are filtered by low pass filters with corner frequency of 50 Hz and with the gradient of -6 (db/oct). Also those on (a) were corrected by dynamic filters, but those on (b) and on (c) were not. These results suggest for the control clock of a routine operation to be sufficient for beam accelerations even at transient regions of P2 and P3. On ripple current, the improvements are very effective. As an example, current ripple of the Qf magnet is given in Fig. 8 under the same circumstances in the Fig. 6 or 7. The ripple estimated at 0.07% on injection and at 0.008% on flat top. Those of B and QD are estimated at 0.03 and 0.08% on inj. and 0.007 and 0.008% on FT.

For a long time stability test, the flat top current of magnets were measured at every period of A typical example, pattern operation on a half day. Fig. 9 shows for the buffered output of current pattern and of DCCT and for the ACR deviation operated by analog,



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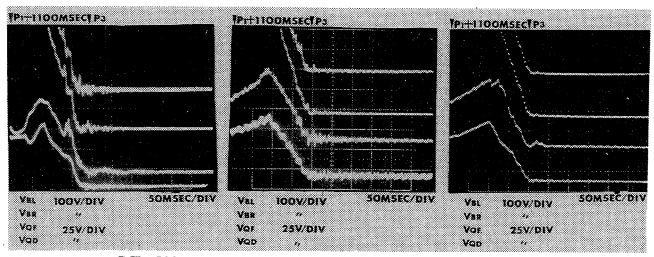
(a)controlled (b)controlled (C)controlled
by H-350 by H-04M by H-04M

Fig. 6 Measured voltages of magnet groups at P2



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(a)controlled (b)controlled (c)controlled
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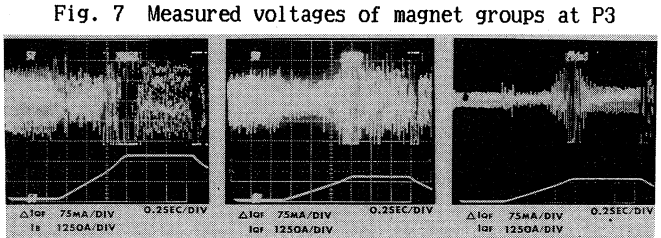
Fig. 7 Measured voltages of magnet groups at P3



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(a)controlled (b)contl. by H-04M (c)contl. by H-04M
by H-350 partially improved present

Fig. 8 Ripple curent of QF magnet

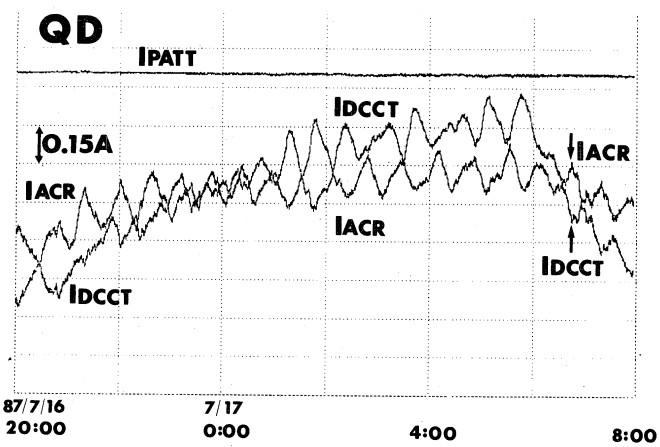

Fig. 9 Typical drift on pattern, measured and deviation of QD magnet current.

sampling at near the center of FT. There are slow frequency component with several tens minutes and the very slow one with a day. These are correlating with the ac line voltage closely. However, these components are not harmful to tune of the beam in the magnitude less than 0.1% , because of the similar quite trend to BPS and QFPS. At present, the current control by the periodic control method is not used in continuous, but used in batch process as in pattern correction of initial generation, because of disturbances on sampling by large jittering on the 600 Hz control clock. As the longer term and over-all stability test, measurements of tune were executed on the same pattern. Fig. 10 gives these data. Vertical tunes with 50 ms step are

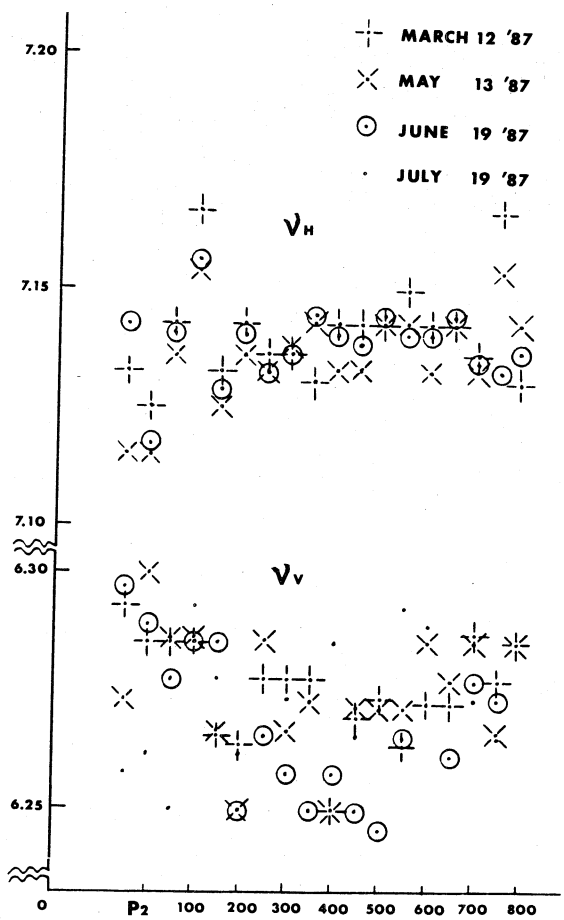

Fig. 10 Measured tune during acceleration on a fixed 12 GeV pattern.

horizontal tunes are within a small variance, but those variances estimated by current ripples are there with a small factor 10 % or less. These differences would be expected to make clear in processes on the control system tuning and optimizing on the PS.

Acknowledgements

The authors would like to express their sincere thanks prof. Michio Nakano (Tokyo Inst. Tech.) for his discussions and many advices on the control system. They would like to describe their thanks to professor Emeritus T. Kamei for his encouragements and supports. They are much indebted to prof. H. Baba, Director of AR, for his advices and discussions on the system construction, Mr. N. Toyama for his measurements of tune and prof. M. Kondoh for his discussions on the project and to many colleagues of PS group for their discussions and collaborations.

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