SOME PROBLEMS ON THE NEW COMPUTER CONTROL SYSTEM FOR THE MAIN RING MAGNET POWER SUPPLY OF 12 GeV PS

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ABSTRACT

Replacing plan of the H-350 system is reported. In the whole analog and digital hybrid system, the control makes the new computer system resposible for the periodic control (a kind of adaptive control) and the analog loops resposible for real time feedback control.

The distributed system consists of three systems of the HD-68000 family. The main carry out the periodic and the other control tasks and background jobs under supervision of UNIX. Input- and output-controller engage in running data log to seven sets of ADC and in pattern data distribution to fifteen sets of DAC in every 1.67ms locked in six phase ac power line. The systems will have been installed at the end of 1960.

INTRODUCTION

Since 1979, the control computer system of dual H-350[1] has been working reliably on routine operations of the main ring magnet power supply (MPS)[2] for the 12 GeV machine. On the other hand, the trial accelerations of polarized and light ion have been taken on the main ring at several times for the last year. But used patterns were not always optimum, because of restrictions by high power apparatus, by analog and by digital control system.

We will make clear on these restrictions and describe a plan replacing to the new computer control system to remove some of them under minimum improvements to analog control system and to power apparatus. And we discuss on the remained problems.

REQUIREMENTS FOR PATTERNS

1. For polarized proton, patterns of bending field B have the time gradient B as large as possible within Bmax. The final beam energy take in from 500 MeV to 12 GeV.

2. For light ions, B patterns have to have multi-steps coresponding to beam energy to rebunch the beam for RF-acceleration[3]. Figure 1 shows a schematic pattern of B.

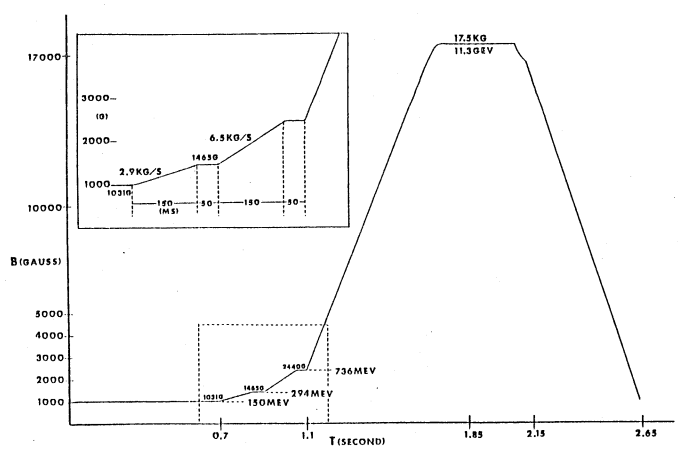

Fig. 1. A Proposed Bending Field Pattern for Light Ion Beam Acceleration.

On these pattern generations including Qf and Qd tracking, the bending magnet power supply (BPS) has the most predominant contribution to complicated correlations among power apparatus and analog and digital control system. Therefore, we describe some problems on the BPS to be overcome for these optimized pattern operations.

SURVEY OF THE RUNNING SYSTEM

Pattern Generation and Periodic Control

The bending magnet power supply (BPS) consists of six groups of 12 pulsed thyristor converter. These groups have power ratings designed for fixed operation modes. For a desired current pulse, the H-350 system calculate the applied voltages to the magnet by every group based on the mode. These voltages are regarded as the reference patterns named Vc, Vi, V23-1, V23-2, V23-3, and V23-4. These patterns have data in every 10 ms. Vc group has a constant value except the magnet reset time interval from beam-ejection-end to next-beam-injection-start with 0 value for bypassing and gives beam injection field in the magnet by adding Vi group of constant inverter voltage. The Vi group compensates ohmic voltage drop between from injection inverter up to ejection coverter voltage. The V23-j (j=1 to 4) have the same pattern ammong the V23 group.

These patterns do not generate the desired current pulse because of neglecting transfer function of dc filters and of minor automatic voltage regulator (MAVR) of every SCR bridge. Periodic control algorithm calculates correction voltage pattern on steady current deviations from a desired current pattern and adds it to Vi pattern. These functions give underdamping characteristics at transient regions of acceleration start and end. The periodic control[4] could not compensate these oscillations within a several times of ripples by correction data interporlated in a quater step between data of every 10ms control clock, though the corrections are effectively improved comparing with the case of single 10ms step.

In the smoothing interval from acceleration to ejection, V23-j groups are controlled serially in group unit, independently on their pattern data, by the timing parameters for the purpose of reducing reactive power within controllable range of reactive power compensator (TQC)[5].

The similar timing controls have applied to the magnet reset time interval. On continuous periodic control, the steady current deviation on the reset start region induces oscillations near-by flat top end by the algorithm. By program maintenance or developments, it might be possible for the oscillation to be suppressed. But, the periodic control has carried out only for the optimization of the reference voltage patterns at a new pattern generation and modification or for drift corrections to automatic current regulator (ACR) deviation by manual control.

As results of timing controls, the voltage patterns are not effective in the interval and for analysis to effective factors to be difficult by very complicated correlations among ac power system and dc components including transient. These irregular controls would be attributed to underestimation of saturation in self-inductance of the bending magnet and to lack of flexibility and processing power of the cpu system. However, as for routine 12 GeV pulse patterns, optimizations have been done in sufficient level to accelerate stably and reliably the beams. But these optimizations needed long time to converge.

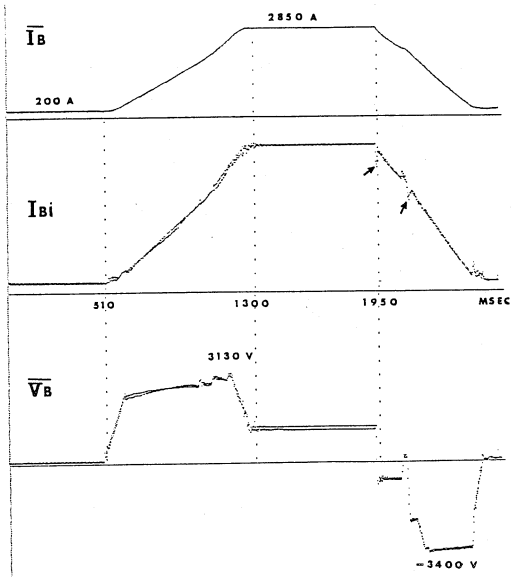

Fig. 2 A Typical Thyristor current of a Bridge on a Routine 12GeV operation.

Extinction of Thyristor Current

One of these correlations is extinction of SCR current, Iscr, in pulse operation of magnets fed by serially connected multi-stage bridges. The extinction would occur at down-step voltage for SCR current to be suppressed by discharge current of capacitors in low pass filter, if Iscr less than holding current. The extincted element is suffered from accumulated over-voltage by the other bridges connected serially and transient voltage oscillations and will break down simultaneously.

Figure 2 gives typical SCR current Ibi of Vi-bridge rectified by 3-phase diode bridge on a routine 12 GeV operation. The maximum current suppression would be estimated at about 400 A on the reset time interval. The similar current suppression may occur at the end of acceleration in non-optimized patterns, especially in adjusting the pattern by timing control. This is the reason for the restriction of flat top current. To guard the element, these transient over-voltages are bypassed by CR-networks, although it is impossible to operate by the patterns which induce a extinction. The networks have been installed last February.

Software Development

The character of the system is in a real time multi-tasking process controller under the standard OS named PMS II. The OS does not support control program development and maintenance except object level. In the cpu, these works are supported at assembler level only by the other OS-NPMS I at off-line, but both OSs are never able to implement at the same time. Usually, like the running control programs, application control programs are developed by assembler and high level FORTRAN like language PCL on an upper version system of the same family, H-500 or H-700, or on a main frame with special tools for the HIDIC-family. But we have not any supporting system. Therefore, the maintenances of control programs were forced to be confined patch level. In pattern generation, desired pattern parameter input by paper tape and the data are checked merely to printed data. Since the last March all of the system family have been manufactured only by a claim as the supply parts for maintenance, including peripherals. In very near future, the system may not be supported in hard- and soft-ware.

In recent developments of microcomputer families and memory elements by LSI technology, reliability and performances of their composed system have been improved up to almost the same level as a mini-computer for process control, like H-350, which constructed by discrete or SSI components. Developments of peripherals have made reasonable circumstances on software works compared with the H-350 system in display, external storage memory and data transfer or communication etc.. These advances suggest for the costs replacing the system to a new powerful microcomputer systems to reduce reasonably, comparing with reconstruction of the H-350 system with developing the system design in software and in hardware to solve problems on the flexible pattern operations.

PROJECT OF NEW COMPUTER CONTROL SYSTEM

System Design Principle

Since most of all the problems would be related on the computer control, the system design is the most important to construct the minimum system in hard- and soft-wares but the maximum in cost performance to our whole analog and digital hybrid system. The analog control system have to play in main role on real time processes. But, it is reasonable for the digital system to be responsible for fast feedforward pattern control and to slow but reliable feedback control loop, periodic control part of ACR. Real time part of ACR transfers to the analog loop with not-expensive cost.

Structure of the control computer system is desirable for these loops to be constructed reasonably by multi-cpu. The main parts of the digital system are constructed from a 16-bit-microprocessor and their family LSI components on a industrial standard bus and supported by universal operating system as the software bus and standard peripherals, commercially available. Under these circumstances, high level language and powerful utilities support development and maintenance of soft-wares for the flexible pattern control with reasonable total cost. The main cpu system controls for the slow loops and supports the other tasks and background jobs. For the fast loop, other cpu systems engage exclusively in tasks of which application programs would be described by assembler.

H-V90/5 System

Figure 3 shows a layout of the new system. The system consists of the main cpu system HIDIC-V90/5 and input and output controller HISEC-04M. The distributed three systems are not hierarchical in software, but rather independent even in assembler level between the main and the controller, because the structure supported only by upper version of H-V90 series. The main components are LSI of HD-68000 cpu (second source of MC-68000) and the family. These have assembled on boards as function module given in rectangular block in Fig. 3.

The system has DRAM of 2MB, standard peripherals (i.e. 5"-20MB hard disc and 8"-2MB floppy disc drive, two stations of CRT terminal, and two printers) and two loops of local area network based on IEEE 802 (LAN 1 and 2). These resources supervised by the main OS compatible with UNIX.

The system is responsible for almost of all controls except fast real time parts undertaken by input and output controllers and to developments and maintenances of control programs and data. The application programs will be descibed in the system language C and FORTRAN 77. The main tasks are the operation controls including start-stop and status monitoring, correction pattern calculation of the periodic control and fine adjustments of pattern data for on-line control. For supporting tasks, the system works on pattern generations, processing of pattern and operation data, control program development, and background processes.

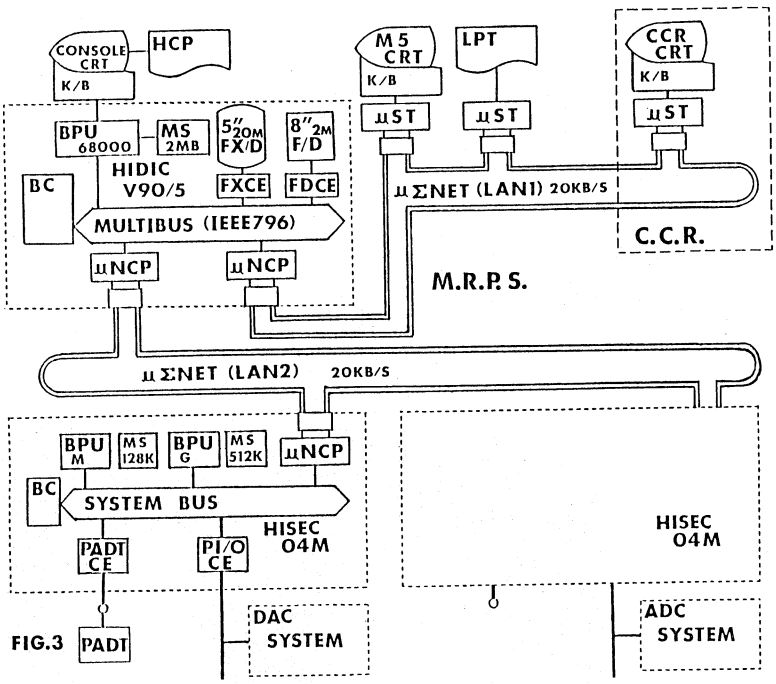

Fig. 3. A Block Diagram of the New Distributed Control Computer System.

The system communicates exclusively the input and the output controller by LAN 2 because of reliability data transfer. The network transfers pattern or logged data between the main and output or input controller by the speed 20 kB/sec corresponding to a quarter of the one of H-350. But, on a fine adjust practical response would not be so slow comparing with every clock transfer of the H-350 because of block transfer and the exclusive path, though the data increased six times as large as those of the H-350.

Controller System

The output controller schedules nine sets of 16-bit-DAC for BPS, that is, six of them serve as reference pattern voltage of the converter group, two as the dynamic filter detector and one as the reference for the analog ACR. Figure 4 shows shematic relation among these hybrid loops for one group 12-pulse converter of BPS and Qf- and Qd-PS. And also 3x2 sets for Qf and Qd. The system outputs these pattern data to the fifteen sets of DAC in every clock of 1.67ms. But the data convert in synchronizing to the zero-cross pulse of six phase ac power line. Bridge control signals of by-pass and gate suppress are distributed to working bridges by the system.

The input controller reads data of seven sets of 16-bit-ADC. Three sets serve for the DCCT current signal and the others for the dc voltage applied to the B-, Qf- and Qd- magnet in the same sampling clock of the DAC system. The clock synchronizes zero-cross pulse perfectly, but has a constant lag of about 100 microsec. At the edge of clock pulse, ADCs have ceased their sampling because they had started synchronizing to the zero cross pulse. These dc voltage data serve as a new periodic control loop for the magnet voltages.

DISCUSSIONS

After the project, we shall have still some problems by the power and control system.

For a flexible pattern control, control of BPS bridges especially those of V23-groups have to be flexible. But the time interval of flat top would be rather determined by the thermal rating of bypass thyristors in V23-bridges, if the flat top currnt was larger than 2000 A within power rating of bridges. These have two elements of the same rating to bridge arm thyristors.

In the transient regions of pulse operation, phase lock control in the power line is important to estimate steady deviations to pattern data for the periodic control. But there are several times larger systematic differnces between phase lock control by up- and down-ward zero cross pulse than those of voltage ripples. In the limit of memory space of controllers, real time control pattern have to choose the one by up- or down-pulse. As a result, jitter between the main ring and the booster PS will be 20ms at the maximum, twice times of the H-350.

These problems would not be fatal to practical operations of PS.

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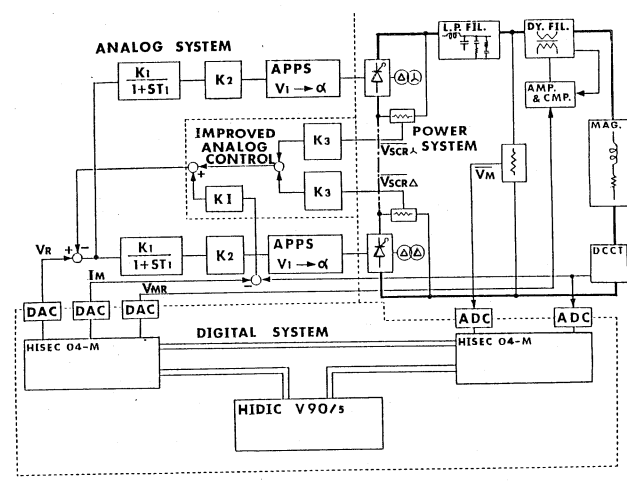

Fig. 4. A Schematic Diagram of the improved Hybrid Control Loops for a 12-Pulsed Converter.