PHOTON FACTORY LINAC RF PHASING COMPUTER CONTROL SYSTEM

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Introduction

The phasing of the 40 high power S-band klystrons of the PF injector will be done under computer control. This is neccessary to optimize the acceleration.[1] Various indirect comparison "Beam Induced" methods for long linacs have been adopted by SLAC[2] and ORSAY[3]. In the Beam Induced method a CW reference (E_{ref}) is first matched in phase with the pulsed RF signal (E_i) induced by the beam in an otherwise empty cavity or waveguide section. Then the klystron is matched to the reference phase. Computer control has been done at SLAC[4].

In the PF linac the low power phase shifters for each klystron are contained in IφA units (Isolation, Phasing, Attenuation) located in each modulator. Since the IφA is controlled by a microprocessor FOCUS was investigated for implementing the entire phasing function there.

Outline of Functional Operation

It turns out phase detection can't be done at the IφA level because of no inputs, the monitor RF signals from the 8 klystron in a sector will be routed directly to the sector control level. The final form that the phase detection will take is still under active investigation, as described in the paper by OSAWA et al. in this conference, and the overall features and design concepts of the linac computer control system are discussed in the paper by NAKAHARA et al. Therefore Fig. 1 shows only the control units involved in phasing.

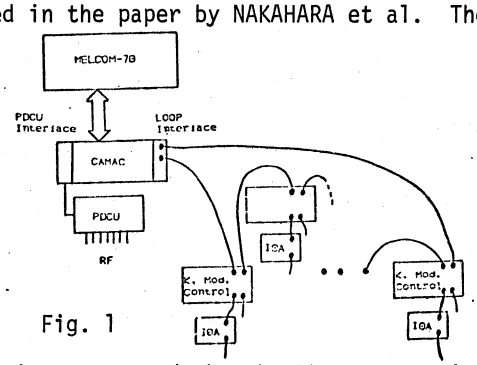

Fig. 1

The actual phase comparisons are made by the Phase Detection Control Unit (PDCU) at the command of the sector control MELCOM-70, and the phase of each klystron is set by its associated IφA. The CAMAC Crate and Klystron Modulator Controller boxes serve merely to carry messages.

Phase Detection Control Unit and IφA

A function diagram of the PDCU is shown Fig. 2. In general this unit is designed to work as independently as possible. Given a "start" command from the MELCOM-70 it first sets up the RF switches and sample timing delays. On the reference adjustment cycle it will control its local phasing unit with a stepper motor-encoder. On the klystron adjustment cycle it will make up command messages for the

klystron IφA unit. Except for a different communication protocall the IφA is just a copy of the part of the PDCU that controls reference phasing.

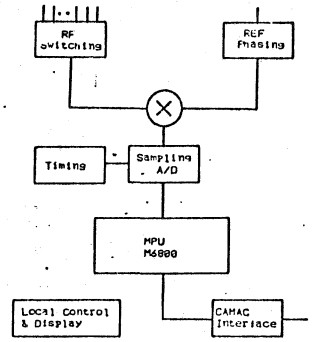

Fig. 2

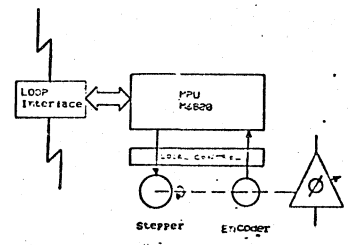

Fig.3

Appendix - Logarithmic Number Systems for Microcomputers

8-bit microprocessors have become cheap enough that they are finding many new applications, but the normal signed binary representation of numbers allows quantization only to the 0.7% level, for phasing this would be 1.4°. For better resolution 16-bit microcomputers are becomming available but slowly and at greater cost, multiple precision arithmetic can be used at slowed execution time and increased storage requirements. A third approach would be a more efficient encoding of the data and this is often done via logarithmic coding.

The primary advantage of all log systems is the great increase in the number of states near the origin, at a proportionate rougher quantization for extreme values. The FOCUS System[5,6] represents numbers by:

$$Y = \text{Sign}(x) \cdot \{ 8 + \log_2|x| \} \quad |x| \leqslant 0.004$$

The outstanding virtue of FOCUS and the system of SWARTZLANDER & ALEXOPOULOS[7] is that the usual 4 arithmetic operations can be defined and implemented efficiently. However the input/output codec transformations are not easily done.

Another important class is that developed by Bell Labs for codecs using for example, the μ=255 Law:

$$Y = \text{Sign}(x) \frac{\ln(1+\mu|x|)}{\ln(1+\mu)} \qquad |x| \leqslant 1$$

This transform is quite robust when the data is more randomly distributed[8] and IC's implementing it either as a stand alone D/A (DAC-76 from PMI) or as a complete telecommunications system[9] are readily available. However, in the transform space it is impossible to define simple operations to implement arithmetic.

Any log system can be effective in relaying digitally a servo loop error signal. FOCUS allows easy implementaion of digital filters at the cost of codec difficulties. μ-Law solves the codec problems at the sacrifice of any possibility of digital processing.

Such systems were rejected for the PDCU-IφA processors for the following reasons: 1) the output of the phase detector is a randomly distributed variable, only the difference between 2 measurements is zero-centered. But the conversion operation is best done by the microprocessor. 2) the conversion from logarithmic representation to the number of drive pulses for stepper motors is too complex to warrant

consideration.

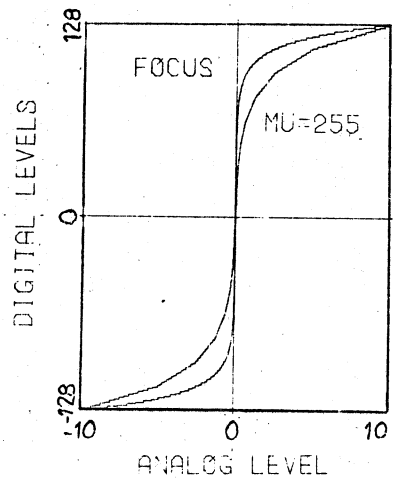

Fig. A1

RFFERENCES

1. H. Herminghaus, "The Effect of Simultaneous Phase Errors and Phase Jitter on the Energy Resolution of Multisection Electron Linacs", in Particle Accelerators, vol 2, pp. 181-184, 1971.
2. H. Hogg, ed. "The Phasing System", pp. 383-409 in "The Standford Two-Mile Accelerator", R. Neal ed, W.A. Benjamin, New York, 1968.
3. P. Brunet et al. "L'Accélérateur Linéaire et sa récente extension", in L'Onde Electrique, vol 49, pp 758-761, 1969.
4. S. Howry and A. Wilmunder, "A Microprocessor Controller for Phasing the Accelerator", in IEEE Trans on Nuclear Science, vol NS-24, pp. 1804-1806, June 1977.
5. S. Lee and A. Edgar, "FOCUS Microcomputer Number System", in "Microcomputer Design and Applications" S. Lee ed. Academic Press, New York, 1977.
6. A. Edgar and S. Lee, "FOCUS MIcro-omputer Number System", in Comm of the ACM, vol 22, pp 166-177, 1979.
7. E. Swartzlander and A. Alexopoulos, "The Sign/Logarithm Number System in IEEE Trans on Computers, vol C-24, pp 1238-1242, 1975.
8. A. Gersho, "Principles of Quantization", in IEEE Trans on Circuits and Systems, vol CAS-25, pp 427-436,z1978.
9. H. Hindin, "Technologies, Architecture Compete for Huge Codec Market", in Electronics, vol 51, pp 105-108, Sep. 14, 1978.