Uniform communication over the MTCA interconnect and network

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Development background around 2010 and my personal view

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Contents

- LLRF controllers at KEK, and MicroTCA
- EPICS at KEK, and “Channel Access Everywhere”
- New (as of 2010) LLRF controller
- RF control configuration

- **Specific (extreme) choice of technology under a certain condition**
  - Usage of GbE only on MTCA

Digital LLRF Controllers at KEK

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- **J-PARC**
  - CompactPCI-based DSP/FPGA system
    - Since ~2003
- **ILC and STF development**
  - Started with CompactPCI-based controller
    - Based on J-PARC experiences
      - Ten 16bit ADC, two 14bit DAC, Virtex2pro
  - ATCA and PLC were chosen for global controls design (2006)
  - ATCA-based controller
    - For ILC "baseline" design large card was required at that time
      - Large card (14bit ADC x "32", 16bit DAC x4, FPGA, etc)
      - Reliability for large number of components
- **Choice of modular system for the future was difficult**
  - VME market/product began to shrink
  - Need reliability (monitoring capability) as well as bus bandwidth
  - No good PCIe based modular system even for cPCI

xTCA and MicroTCA (μTCA)

- **ATCA (2003)**
  - New computing standard for telecommunication and industry
    - After CompactPCI (1993)
  - Many serial interconnects on backplane
    - 2.5Gbps each (10Gbps in the future)
  - IPMI surveillance/remote-management for reliability
- **AMC** (Advanced Mezzanine Card for ATCA)
  - Serial interconnects, IPMI, good part of ATCA
- **MicroTCA (2008)**
  - AMC card itself is powerful
  - Direct slot-in AMC cards in a Box
- **MicroTCA for LLRF should be a good choice**

New LLRF Controller at KEK

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- **cERL (Compact Energy Recovery Linac (Test Facility))**
  - CW, under construction, for future ERL
  - **AMC or MicroTCA-based LLRF Controller**
    - Future stability of 0.01% in amplitude, 0.01degree in phase
    - For now, 0.1% in amplitude, 0.1degree in phase, 1μs loop delay
- **SuperKEKB**
  - CW, under designing, starting part of construction
  - For higher luminosity, higher stability and feedback capability is required
  - Synergy between projects - MicroTCA
- **STF/ILC for S1 global etc.**
  - ATCA control
    - For Clustered RF scheme
  - New RF system configuration , “DRFS” (Distributed RF Scheme)
    - For single tunnel scheme
  - MicroTCA became adequate as well

General Control Progress at KEK (my view)

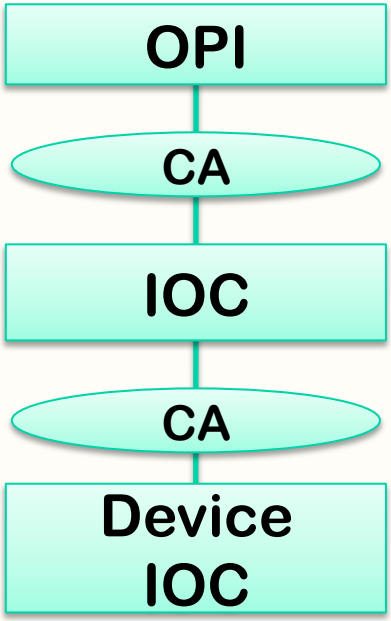
- **VME + Unix (1990~)**
  - Several generations of reliability management cards

- **Every controller on IP network (1993~)**

- **Every controller with EPICS IOC (2005~)**
  - **Channel Access everywhere (CA Everywhere)**
    - Good for rapid development and smooth maintenance

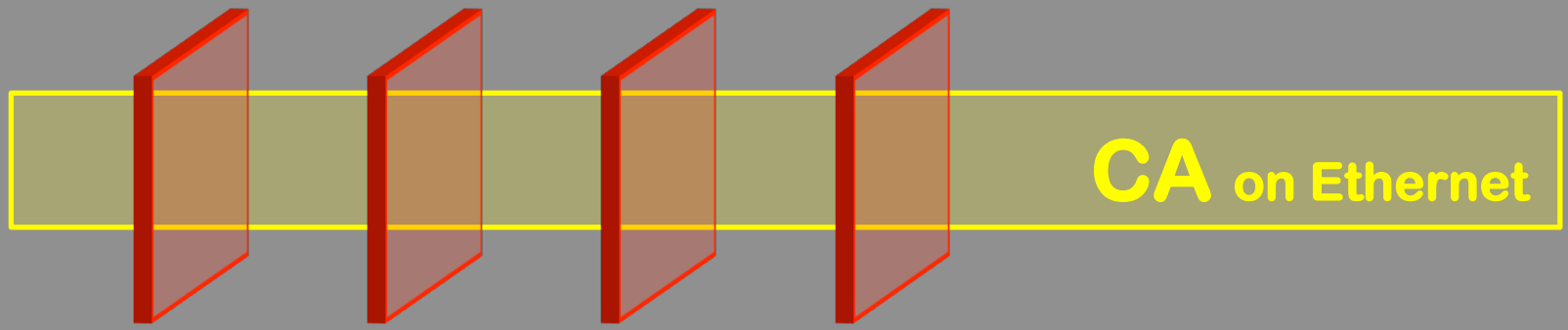
"Channel Access Everywhere"

- **The same software framework on every controller**
  - Rapid development and smooth maintenance
- **Embedded EPICS IOCs at (Super)KEKB**
  - Yokogawa PLC : Linux CPU
  - Oscilloscope 50Hz measurement : Windows
  - MPS management : Linux/FPGA
  - Power modulator : Linux/FPGA
  - Libera singlepass BPM at 50Hz : Linux/FPGA
  - NI cRIO : CAS/FPGA
  - Many more…



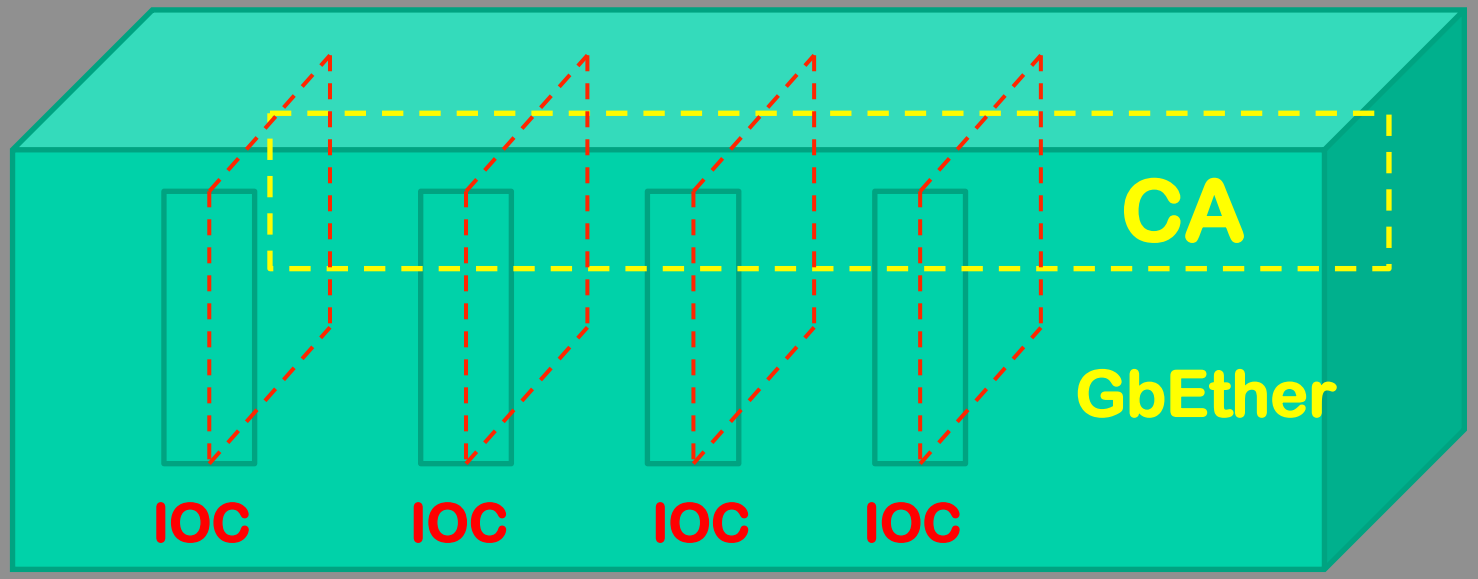
Standard EPICS

EPICS Channel Access (CA) as "Software bus"



Channel Access on MicroTCA Backplane

CA on Hardware "bus"



MicroTCA box

Picture by J.Odagiri

IOC on MicroTCA

- Natural to put IOC on μTCA LLRF Controller
  - Shared among STF, cERL, and SuperKEKB
- Chose GbEthernet as a main media on the backplane interconnect
  - Link to global control is straightforward
  - Not much communication needed between LLRF controllers
    - No CPU cards were necessary
- Chose PowerPC core on Xilinx Virtex5
  - ML507 of Xilinx as a good reference
- Linux on PowerPC
  - Running IOC software to connect to global controls
  - All the fast feedback controls are on FPGA

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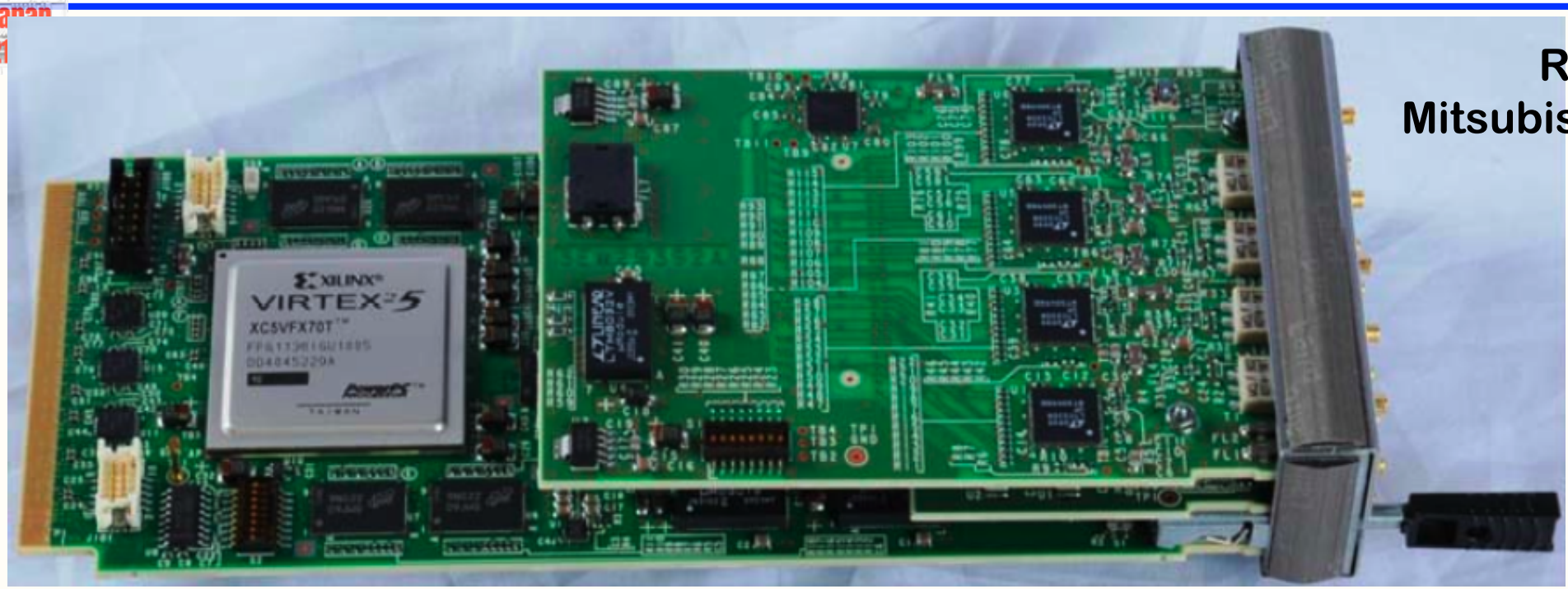
MicroTCA based LLRF Controller

- Single-width full-height module
- Without physics experiment extension (MTCA.4)
  - We started earlier
  - Front-panel connectors only (rather busy)
- Digital part and Analog part are on isolated PC cards
  - ADC 16bit, 130Msps, x4
  - DAC 16bit, 500Msps, x4
  - Virtex5 with PPC440
  - RAM 640MB, Flash 64MB
  - Also monitor card employing the same digital part
    - ADC 14bit, 400Msps, 1.4GHz, x2
- Fabrication was performed at Mitsubishi Electric Tokki System

<http://www-linac.kek.jp/cont/epics/mtca/>



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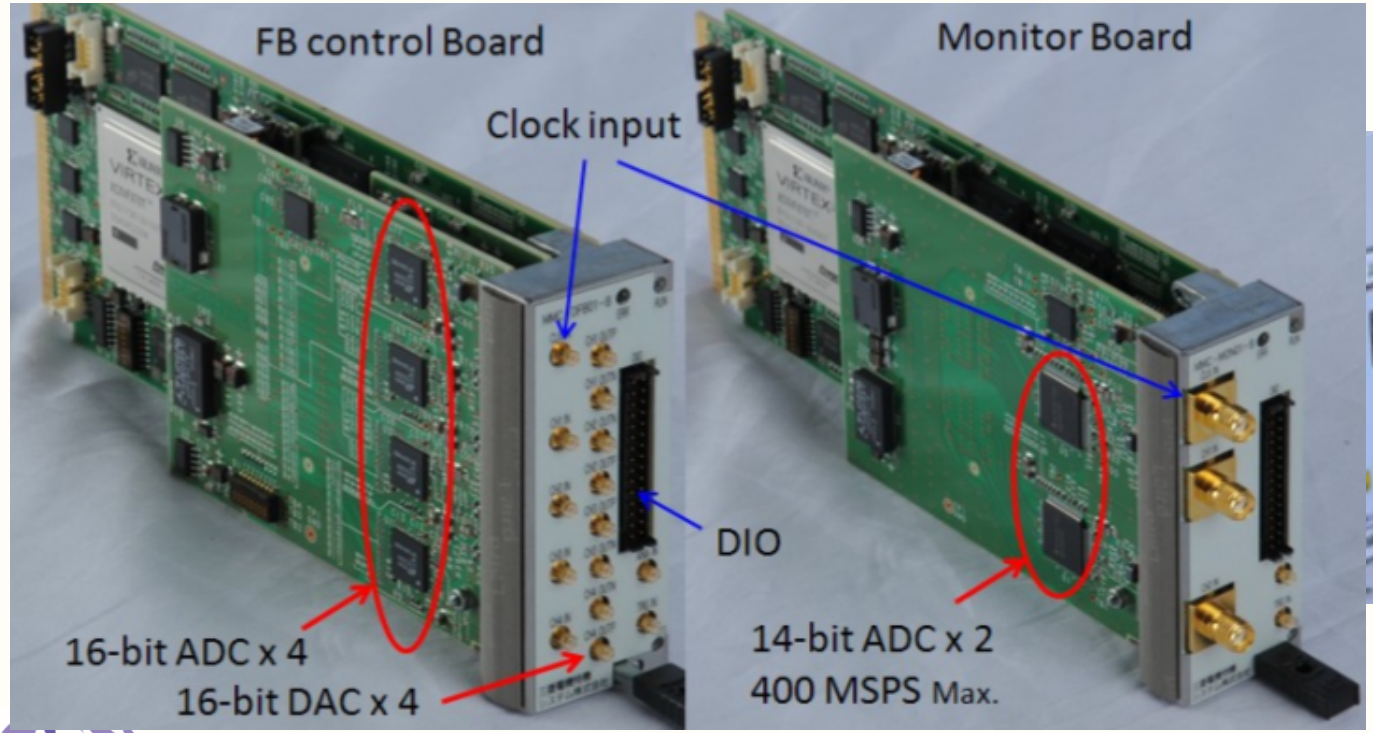
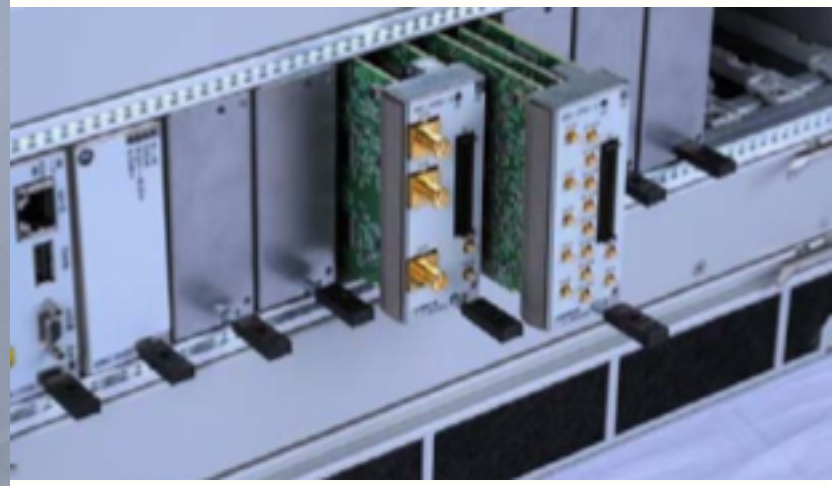
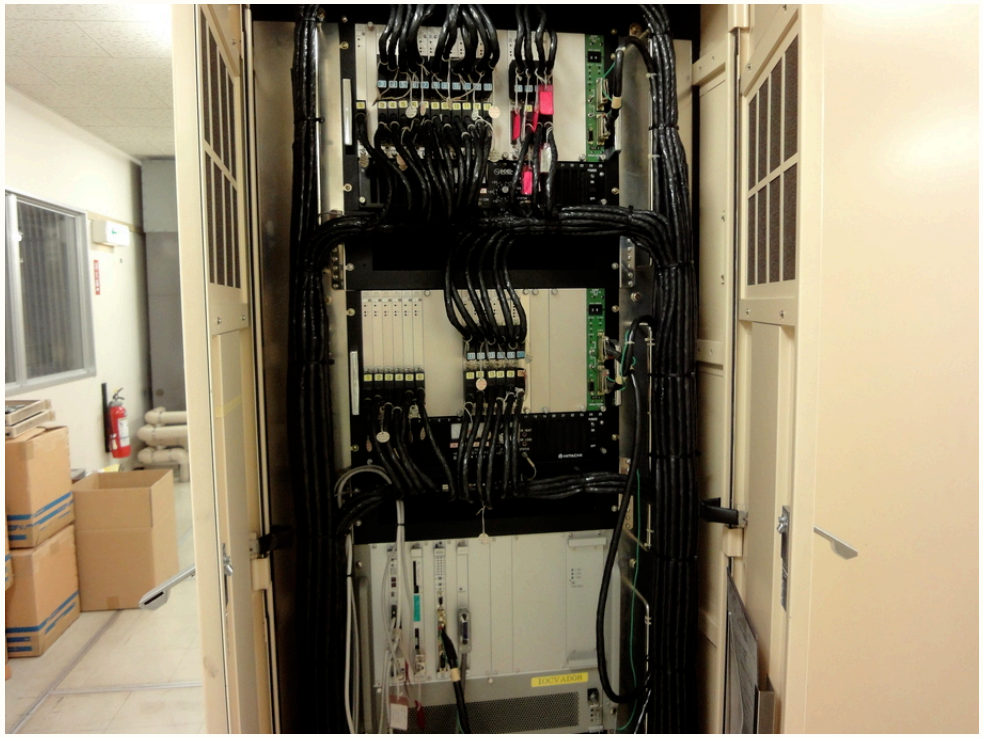
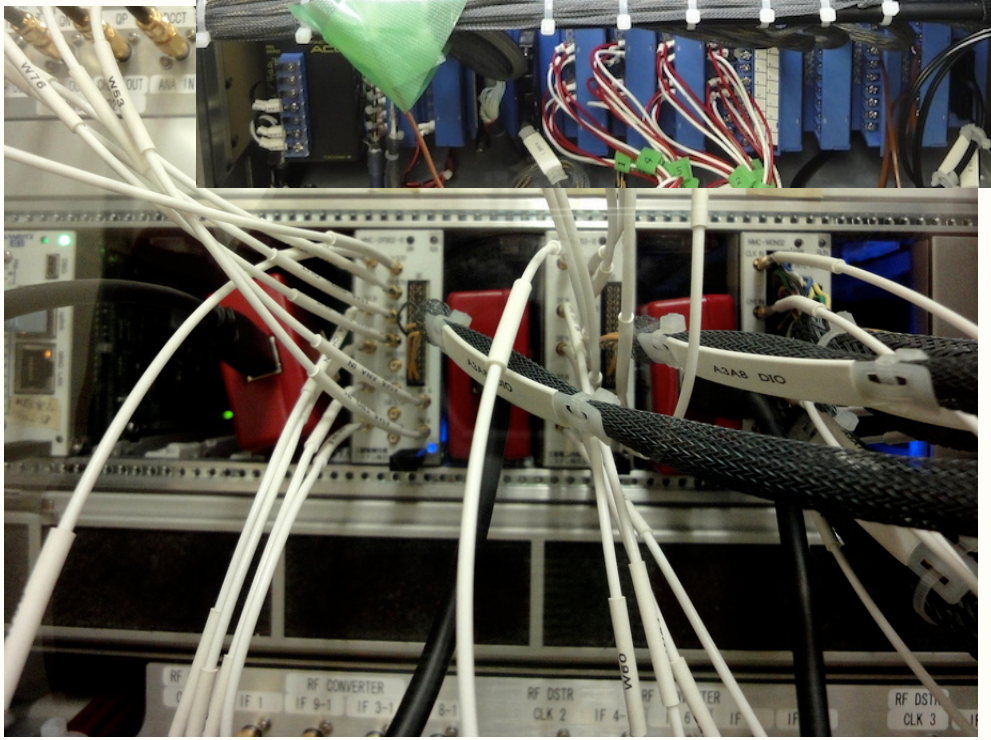
Mitsubishi Tokki





RF Controls



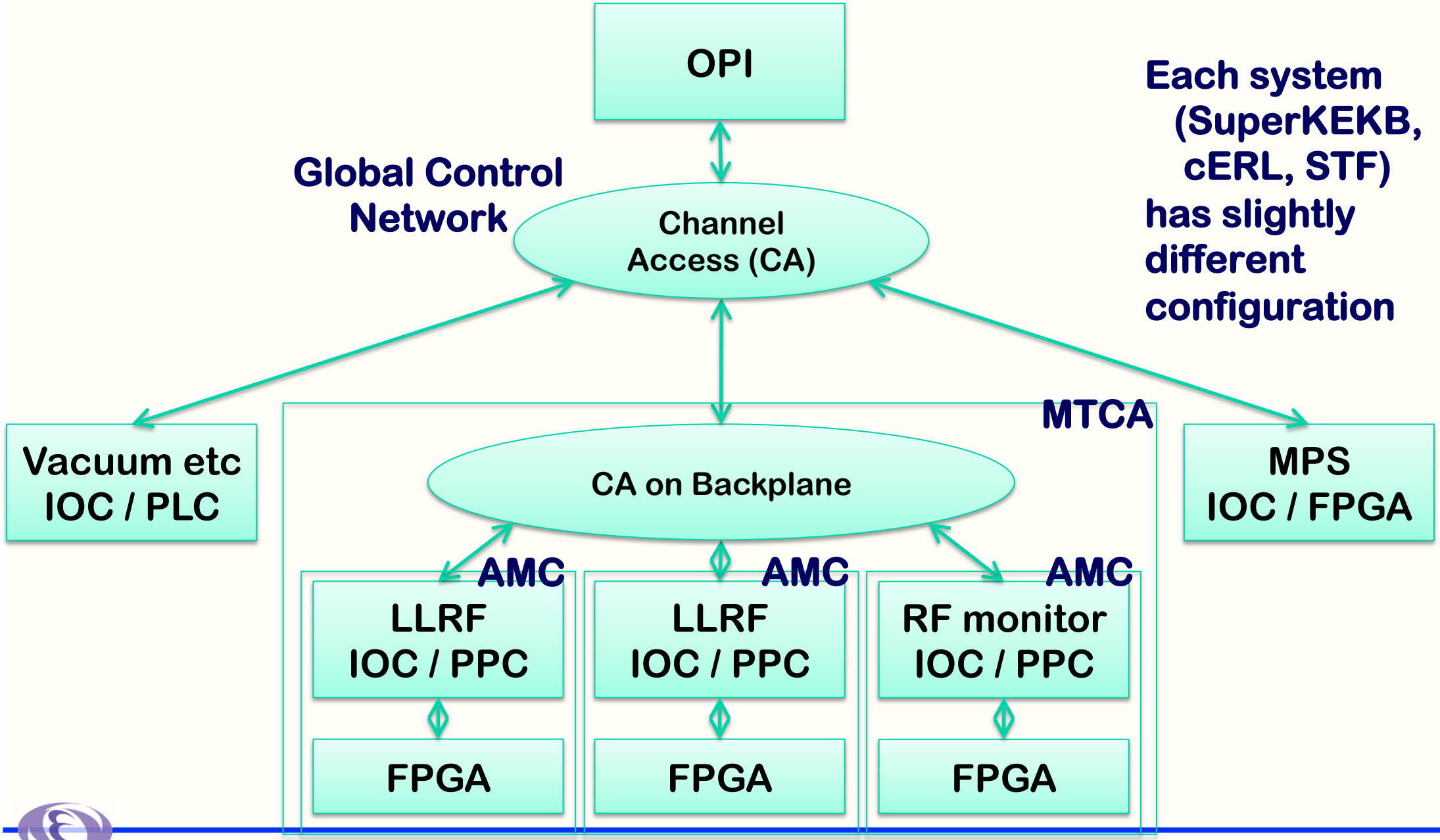


CAMAC and NIM modules

gradually

MicroTCA and PLC

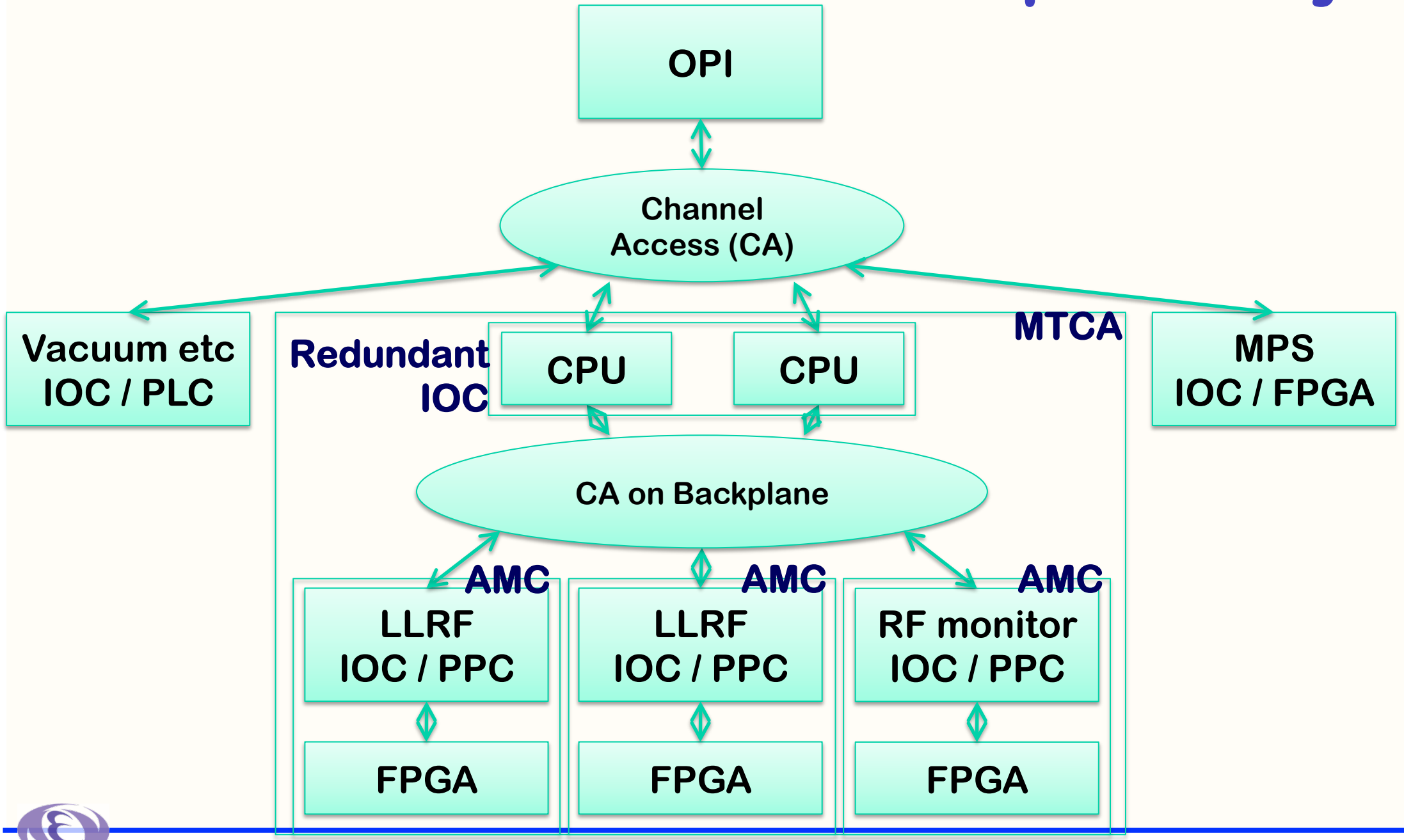
Control Architecture – EPICS Channel Access Everywhere



MicroTCA Management Capability

- For now, we do not depend on the shelf management facility much
  - We do not depend on a CPU card !
- Separately, redundancy of power supply, MCH, CPU, are evaluated, and redundant EPICS IOC will be combined
  - Based on the development with ATCA in 2007 for ILC

Control Architecture – future possibility



Development Projects

- Base hardware/software were evaluated
- FPGA and EPICS (mostly SNL sequencer) application programs were evaluated
- Operator interfaces via standard EPICS tools
  - EDM at first, moving towards CSS
- Commissioned in 2011-2012 for STF & cERL
- Commissioned in ~2014 for SuperKEKB

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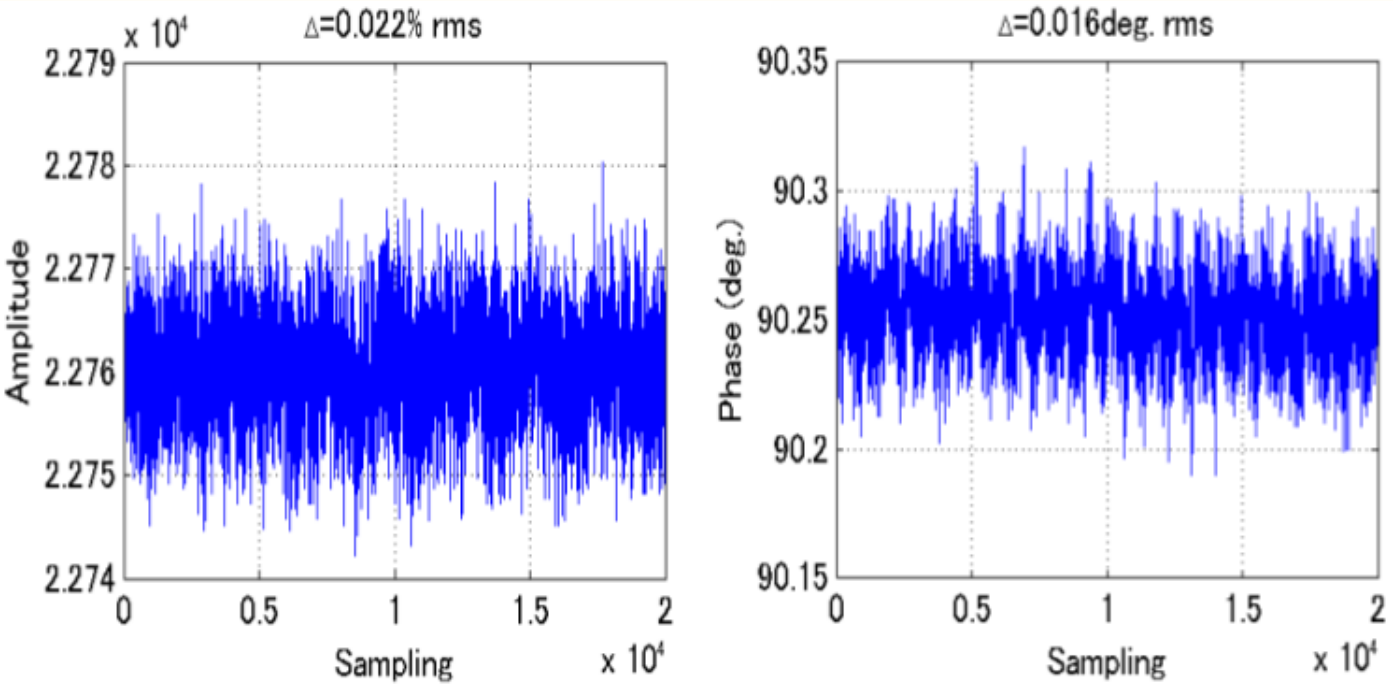
Under Evaluation

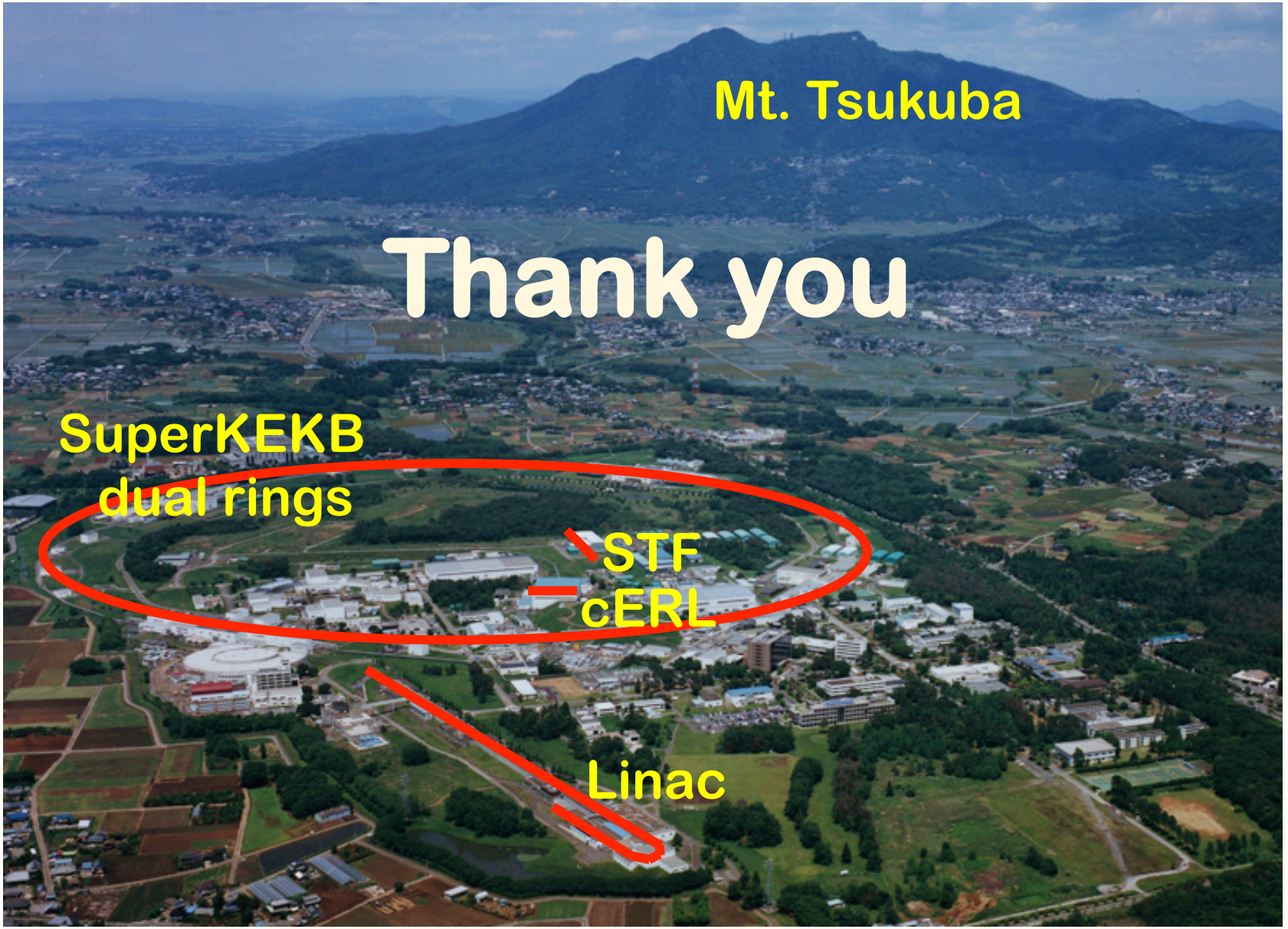
- **Preliminary I/Q control stability results**
  - **Much better than the specification**
    - **~0.022% in amplitude, ~0.016degree in phase**



Summary

- As a natural consequence of several developments (VME, cPCI, ATCA, PXI) at KEK,
  - LLRF controller for MicroTCA
  - with Channel Access (GbE) on the backplane

  was developed
  - All components embed EPICS/IOC
    - μTCA FPGA controller, PLC controller, MPS controller
- showed excellent performance
- was applied for SuperKEKB, cERL, and STF at KEK, as well as other facilities


Mt. Tsukuba
Thank you
SuperKEKB
dual rings
STF
cERL
Linac

Thank you