



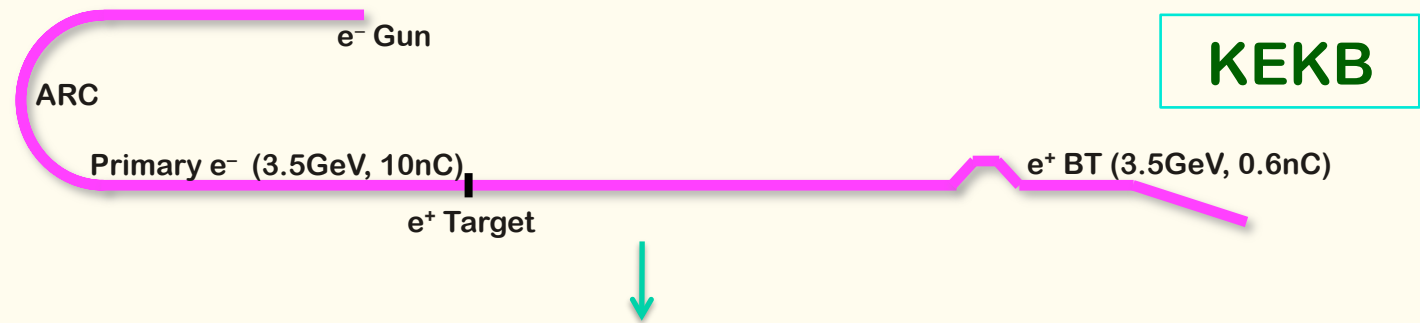
Possible Damping Ring Timing

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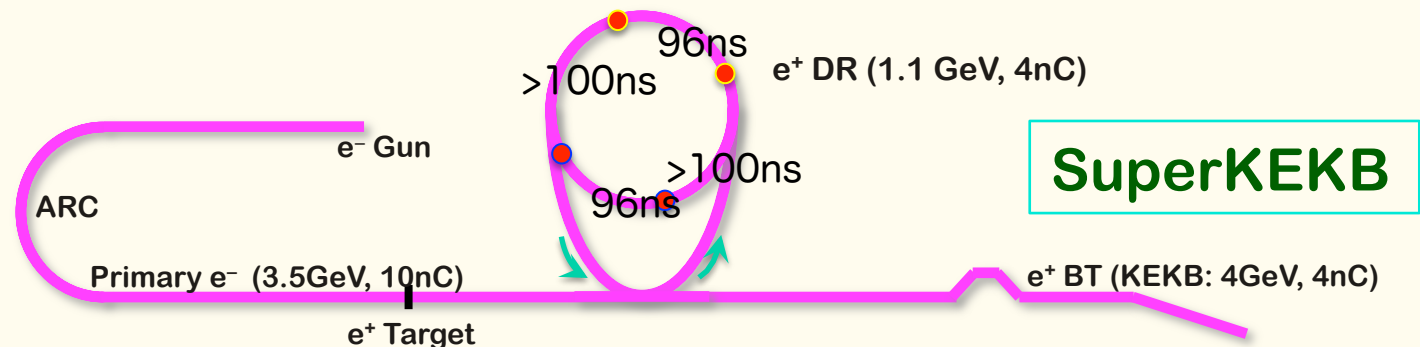
Some info at <<http://www-linac.kek.jp/cont/epics/event/>>
Conference papers at <<http://www-linac.kek.jp/linac/>>

Bucket selection in Phase-2 with DR

- ◆ Without DR, simply wait up to $5120 \times 96 \text{ ns} \sim 490 \mu\text{s}$
 - ❖ 96 ns : highest common frequency between linac – ring



- ◆ With DR, in order to select arbitrary bucket in MR, have to wait up to $\sim 4.5 \text{ ms}$, even if a bucket in DR was carefully selected
 - ❖ Power supply can wait only 2 ms, one of only 2798 buckets in 5120 buckets can be selected, may have to change LLRF condition at latter half of linac every pulse



- ❖ Can be a big challenge in LLRF precision

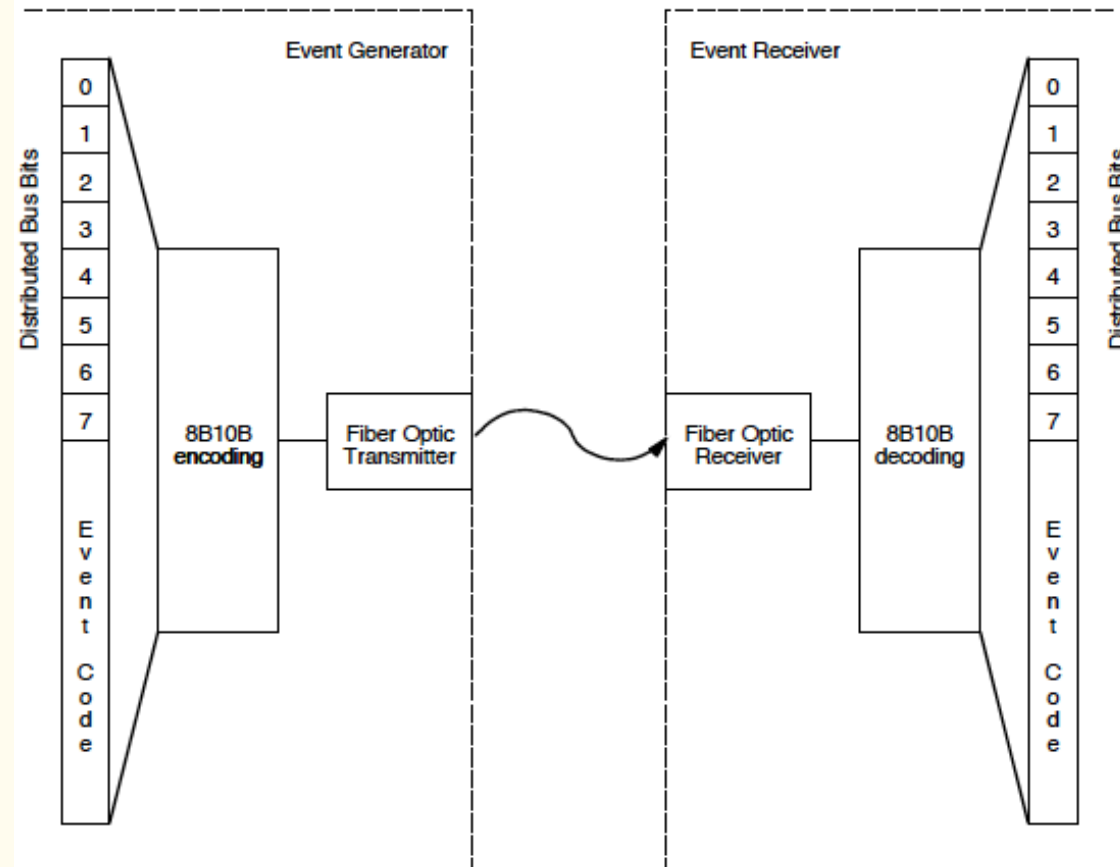
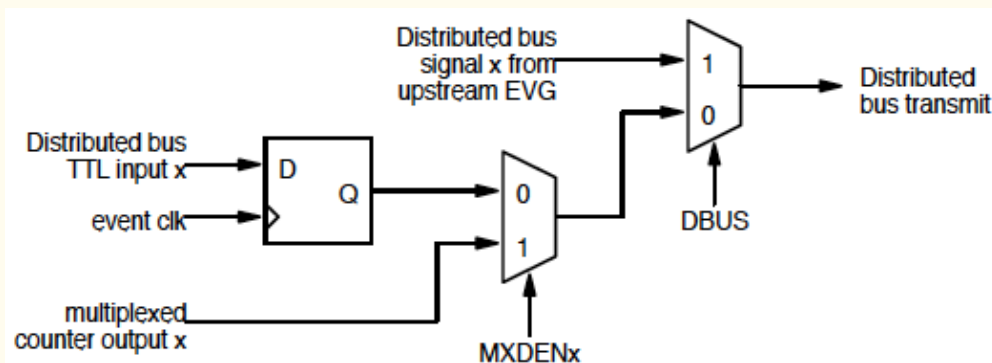
Memo from Oct.6.2016

- ◆ 32k 周 14ms 分記録
- ◆ 読み出しは 12 枚で 0.5秒
- ◆ 2ns または 4ns step
- ◆ Bunch 同期信号、入射 Kicker を打ってから Revolution で Timing を打ち続ける
 - ❖ 20% の Duty 比、TTL
 - ❖ 入射 Kicker が打ったらそれに同期する、つまり 2 pulse 溜めたときには、最初の pulse は無視
 - ✧ ???
- ◆ Start 信号、入射 Kicker から、(NIM)/TTL
- ◆ さらに Revolution を一ヶ所 2 種類
 - ❖ 一つは MR RF から作った DR Revolution と DR RF から作った DR Revolution の 2 つ
 - ❖ 入出射 Kicker / BPM EVR で一方の Revolution を作れば良い
 - ❖ 15 slot VME64x x2箱
- ◆ Dispersion 測定のために 509 MHz を振る
 - ❖ +/- 50kHz
- ◆ そのため、Linac 同期の 509 MHz/Revolution は使えない
- ◆ おそらく Main event system とは切り離れた
 - ❖ Event system または新規開発信号分配 System が必要
- ◆ Dispersion 測定後に出射 Kicker を同期できるか不明
 - ❖ その場合はその独立 Event System 側が出射 Kicker を打つ
 - ❖ Kicker 側は 親 Event system と独立 Event system の双方から Kicker signal を受ければ良い

Distributed bus and multiplexed counters

- ◆ The distributed bus allows transmission of eight simultaneous signals with the event clock rate time resolution (10 ns at 100 MHz event clock rate). The source for distributed bus signals may come from an external source or the signals may be generated with programmable multiplexed counters (MXC) inside the event generator.

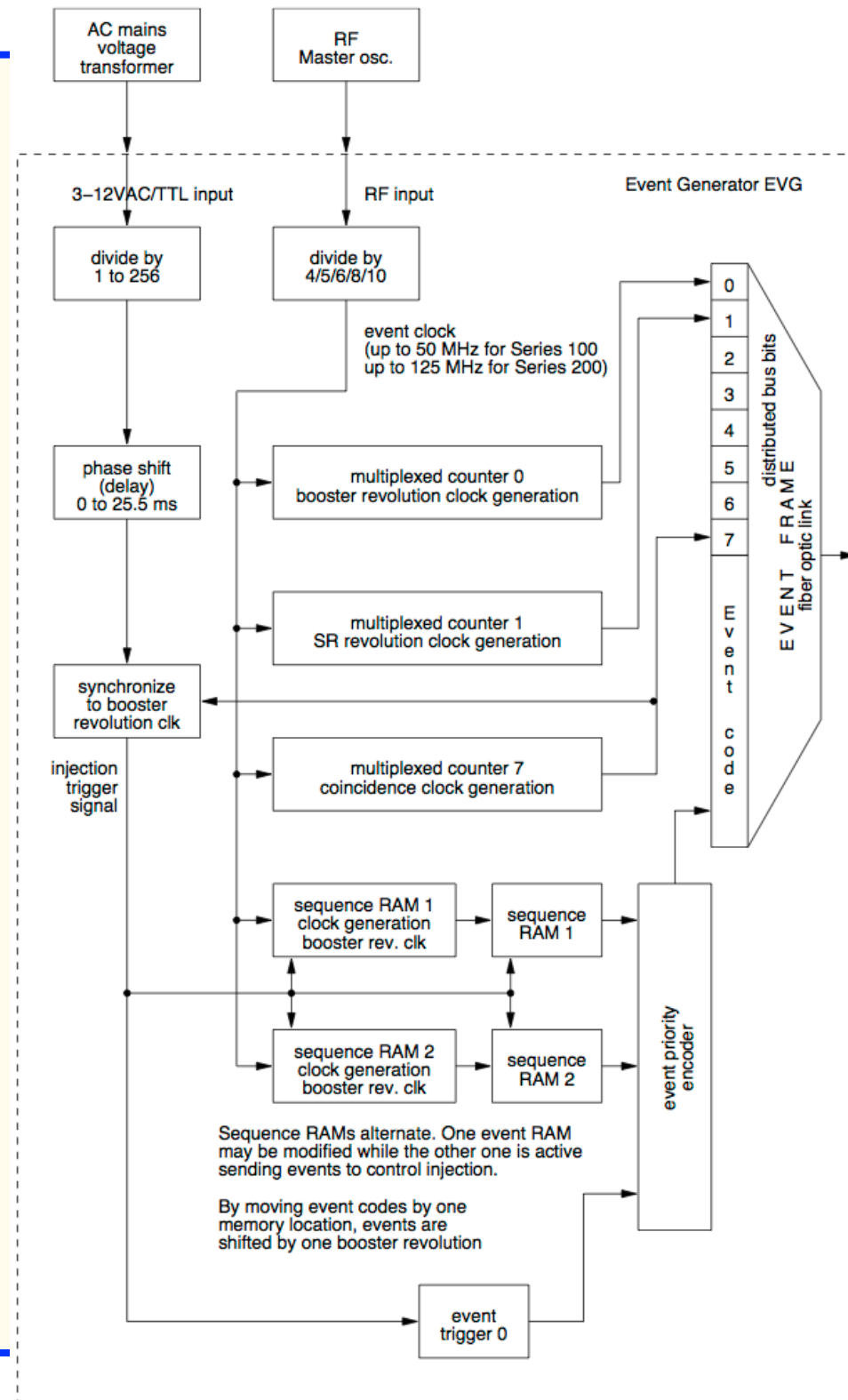
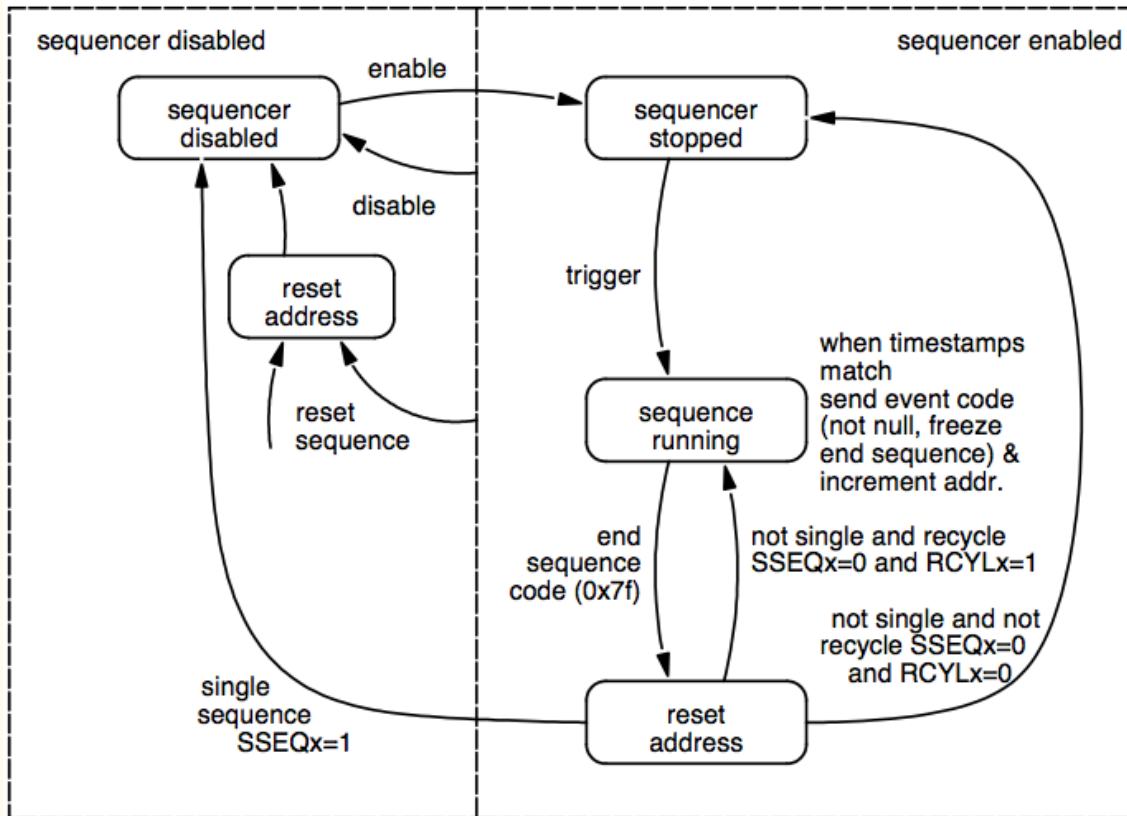
The distributed bus signals may be programmed to be available as hardware outputs on the event receiver.

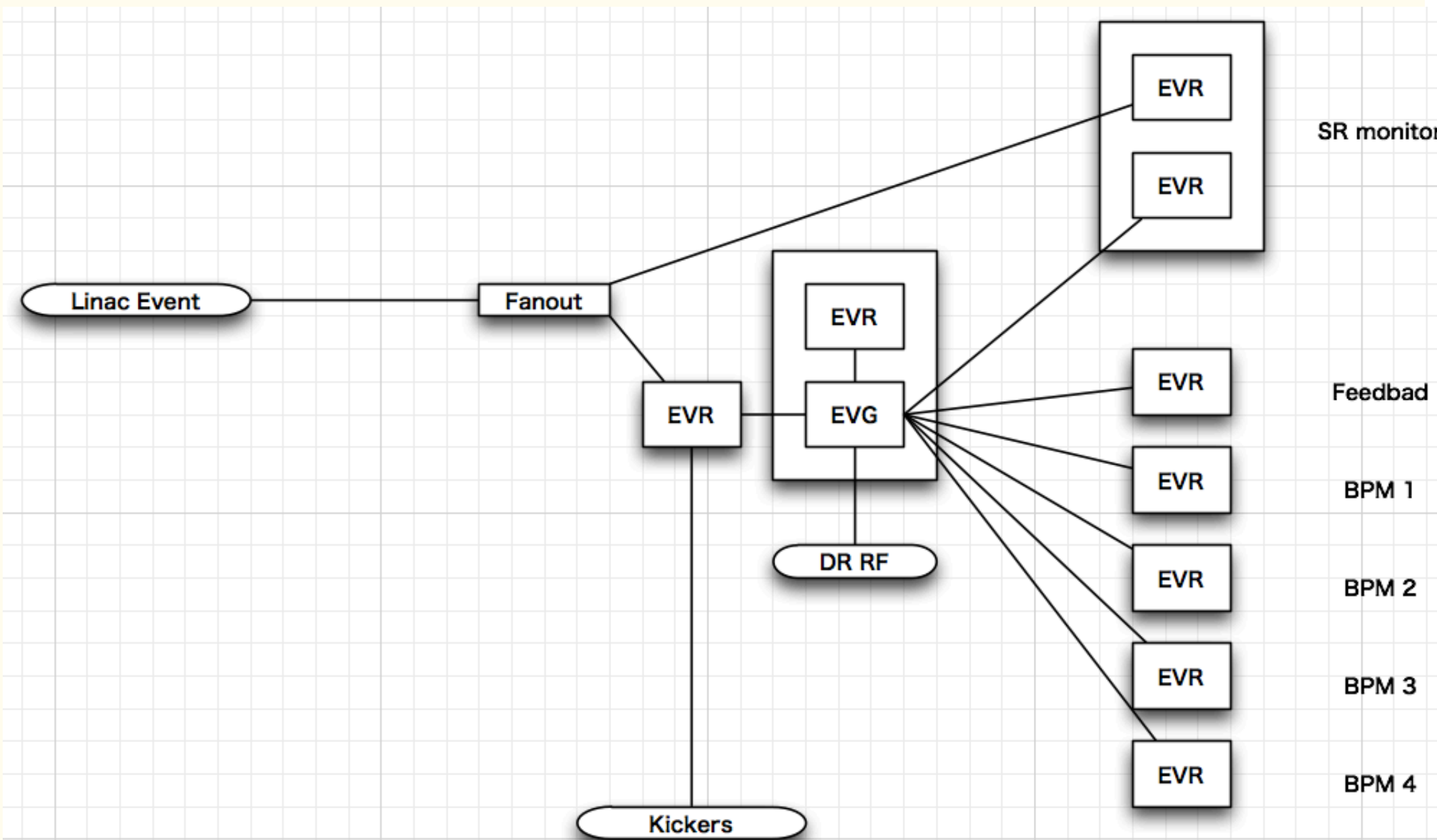




MXC and Sequencer

◆ The end sequence code 0x7f resets the sequencer RAM table address and timestamp register and depending on configuration bits, disables the sequencer (single sequence, $SQxSNG=1$) or restarts the sequence either immediately (recycle sequence, $SQxREC=1$) or waits for a new trigger ($SQxREC=0$).







Pulse-to-pulse modulation

◆ Four PPM virtual accelerators for SuperKEKB project

Based on Dual-tier controls with EPICS and event-system

Independent parameter sets for each VA (20ms)
>200 parameters
for equipment controls
many more
for beam controls

maybe with additional PPM VA of stealth beam for measurement

