

THE PERFORMANCE TEST OF F3RP61 AND ITS APPLICATIONS IN CSNS EXPERIMENTAL CONTROL SYSTEM

Jian Zhuang^{#1,2,3}, Kejun Zhu^{1,3}, Yuanping Chu^{1,3}, Jiajie Li¹, Lei Hu¹, Dapeng Jin^{1,3}
 Institute of High Energy Physics¹
 Graduate University of Chinese Academy of Sciences²
 State Key Laboratory of Particle Detection and Electronics³

Introduction

- The CSNS experimental control system is divided into 3 layers, including front control layer, local control layer and global control layer. Global control layer and local control layer are based on EPICS software.
- In CSNS Experimental Control System, YOKOGAWA PLC will be adopted as controller in device control layer.
- We want to integrate PLC and IOC into one controller to improve system reliability and availability and reduce cost.

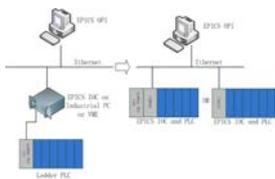


Figure 1: Simplify the path from front control to global control. After Simplifying, reliability increase while cost much fewer.

Net performance test

All results are obtained with Netperf.

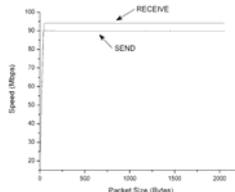


Figure 5: The net speed of F3RP61.

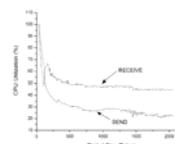


Figure 6: CPU Utilization of sending and receiving

Figure 6 illustrate the CPU occupation with packet size. In this figure, the speed of net increases with the packet size increasing, while the CPU occupation decreases. This effect is caused by the different packing and unpacking cost in TCP/IP stack in different packet size. In control system, the small size packet is dominated, so the net task will acquire more CPU time. And also from figure 6, as more interruption happens, receive task costs more CPU time than send task.

F3RP61 AND Test Environment

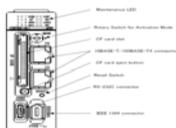


Figure 2 F3RP61

Test Environment

- DELL Optiplex 380MT/SLC 5.4
- Yokogawa F3RP61-21
- Cisco 3750 Switch

CPU Benchmark

Nbench benchmark is used in performance test to known RP61 CPU well. MEM index is for processor bus, cache efficiency and memory performance. INT is integer computing capability of processor. FP is double float performance of CPU. All these expose the theoretical upper limit of the CPU.

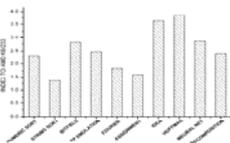


Figure 3: Ten reference program performance Index of Nbench Program Set.

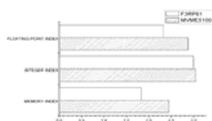


Figure 4: Performance Index Comparison .F3RP61 vs MVME5100

- The results of Nbench on RP61 are showed in figure 2. These results show that, comparing to AMD K6/233, computing intensive kind of program gain more accelerating.
- Figure 3 shows the performance comparison between RP61 and MVME5100, a widely used single board computer in physics experiment and accelerator. Nbench test shows, for CPU capability, CPU performance of F3RP61 is closed to the MVME5100. This means that comparing to traditional ladder CPU, F3RP61 have advantages in compute-intensive applications. RP61 can do some more complex computing task, such as advanced PID algorithm.

CA Access Time

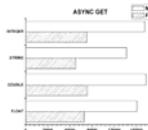


Figure 7: Asynchronous read performance comparison, MVME5100 vs. F3RP61

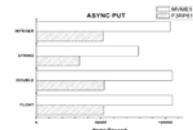


Figure 8: Asynchronous Write performance comparison, MVME5100 vs. F3RP61

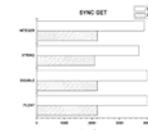


Figure 9: Synchronous read performance comparison, MVME5100 vs. F3RP61

EPICS IOC performance on F3RP61 can be estimated through PV access speed test. Figure 7, 8, 9 shows F3RP61 PV access speed comparing to MVME5100. In this test, F3RP61 and Dell PC are connected in the same CISCO 3750 switch. F3RP61 can provide about one half PV access of MVME5100 in case of full CPU occupation.

Stability of Scan Period

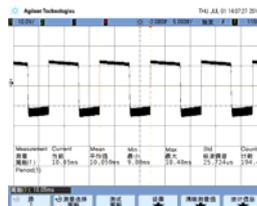


Figure 10: Jitter of 10ms period scan

Figure 10 depicts the output of IOC period scan on F3RP61. The scan period in this chart is 5ms, and the On-Off period is 10ms. After more than 190,000 samples, the Std. Dev. of scan period is about 26us. The Max-min jitter is about 600us. For the general control task, the typical period is about tens of ms. This deviation can be neglected.

Reference

- A. Uchiyama et al. "Development of Embedded EPICS on F3RP61-2L", Proc of PCAAC2008, Ljubljana, Slovenia, Oct. 2008, pp.145-147
- J. Odagiri et al., "Application of EPICS on F3RP61 to Accelerator Control", Proc of ICALEPCS2009, Kobe, Japan, Oct. 2009, pp.916-918,
- <http://www.tux.org/~mayer/linux/bmark.html>
- <http://www.netperf.org/netperf/>
- RTOS-CPU module(F3RP61) Linux BSP Reference Manual, Yokogawa, Japan
- RTOS-CPU Module (F3RP61) Hardware Instruction Manual, Yokogawa, Japan

Summary

F3RP61 can be used as information exchange and control node in the target and instruments control system of CSNS. Now, F3RP61 is used and long-term tested in Function test system with the heavy water control simulation involved in.

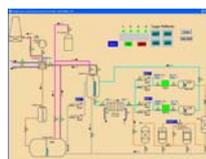


Figure 11: Function test system involving F3RP61 as a controller