THE PERFORMANCE TEST OF F3RP61 AND ITS APPLICATIONS IN CSNS EXPERIMENTAL CONTROL SYSTEM*

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Abstract

F3RP61 is an embedded PLC CPU module developed by Yokogawa, Japan. It is based on PowerPC 8347 platform. Linux and EPICS can run on it. We do some tests on this device, including CPU performance, network performance, CA access time and scan time stability of EPICS. We also compare F3RP61 with MVME5100, which is most used IOC in BEPCII and BESIII. After this tests and comparison, the performance and capability and role of F3RP61 in CSNS (China Spallation Neutron Source) experimental control system is clear. It can be used as communication nodes between device control layer and global layer. And in some cases, F3RP61 also has the capability to exert more functions such as control tasks.

INTRODUCTION TO TARGET AND INSTRUMENTS OF CSNS

Neutron scattering is a powerful method to probe the structure of the microscopic world, becoming a complementary technique to x-ray in the advanced researches in physics, chemistry, biology, life science, material science, new energy, as well as in other applications. To meet the increasing demands from user community, China decided to build a world-class spallation neutron source, called CSNS. It can provide users a neutron scattering platform with high flux, wide wavelength range and high efficiency. The pulsed-beam feature allows studies not only on the static structure but also the dynamic mechanisms of the microscopic world.

CSNS mainly consists of an H- linac and a proton rapid cycling synchrotron. It is designed to accelerate proton beam pulses to 1.6 GeV kinetic energy at 25 Hz repetition rate. Proton pulses strike a solid metal target to produce spallation neutrons.

The high-energy proton beam extracted from the accelerator bombards on the target to generate neutrons through spallation reaction.

INTRODUCTION TO CONTROL SYSTEM OF TARGET AND INSTRUMENTS

The control system of Target and Instruments provides global control and monitor to all sub-system in Target and Instruments division.

The control system is divided into 3 layers, including front control layer, local control layer and global control layer. Global control layer and local control layer are based on EPICS software. In CSNS Experimental Control System, YOKOGAWA PLC will be adopted as controller in device control layer. EPICS is a SCADA software widely used in large scale physical experiment and accelerator.

Traditionally, device controller in front control layer is a ladder PLC. Control logic is running in this ladder PLC. A soft IOC based on industrial PC is used to connect global control layer based on EPICS and ladder PLC in front control layer. This soft IOC exchanges information only. Because of using two cascaded controller, this system structure decreases the system reliability and costs a lot. A nature idea that these two controllers are combined into one is coming out.

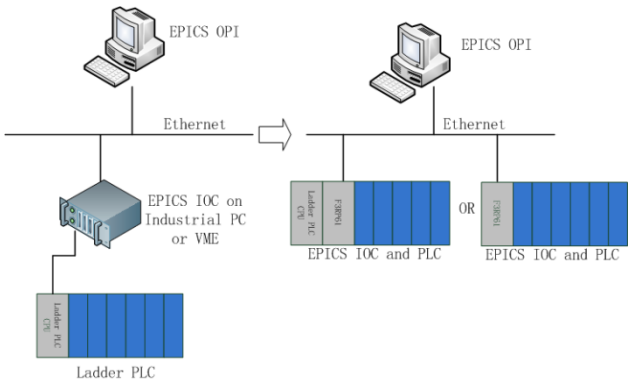

Figure 1: Simplify the path from front control to global control. After Simplifying, reliability increase while cost much fewer.

Now, a new PLC (Programmable Logic Controller) CPU module based on linux OS from YOKOGAWA, F3RP61 [1] [2] [3] [4] [5] [6] [7] [8] [9] [10] [11], began to be applied in larger physics plant. F3RP61 can be used as EPICS IOC with traditionally ladder PLC CPU in the same framework or even replace the ladder CPU. In way of F3RP61 running in same framework of ladder PLC CPU, the cost of switch and linking cable is saved. In case of F3RP61 replacing ladder CPU, the control logic is running in F3RP61. It can use almost all F3 I/O module directly.This saves the cost of ladder PLC CPU further.

F3RP61 will be used as information exchange and control node in CSNS Experimental Control System. The performance of F3RP61 is the important to design the whole control system.

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INTRODUCTION TO RP61 PLC MODULE AND TEST ENVIRONMENT

F3RP61

F3RP61 [14][15] from YOKOGAWA is based on POWERPC MPC8347 533MHz processor. MPC8347 is an E300 core Soc from Freescale Inc. MPC8347 integrates DDR controller, two 100BaseT Ethernet, USB, serial, and mini PCI interface.

Test Environment

All the tests are done on Yokogawa F3RP61-21. The os is linux-2.6.24.3; c compiler is gcc-3.4.3, and libc is libc-2.3.4. RootFs is on Scandisk 2G CF card in the F3RP61. A Dell PC running scientific linux CERN 4.7 is connect to F3RP61 with Cisco 3750 switch. This Dell PC is used as consol host and communication pair of F3RP61.

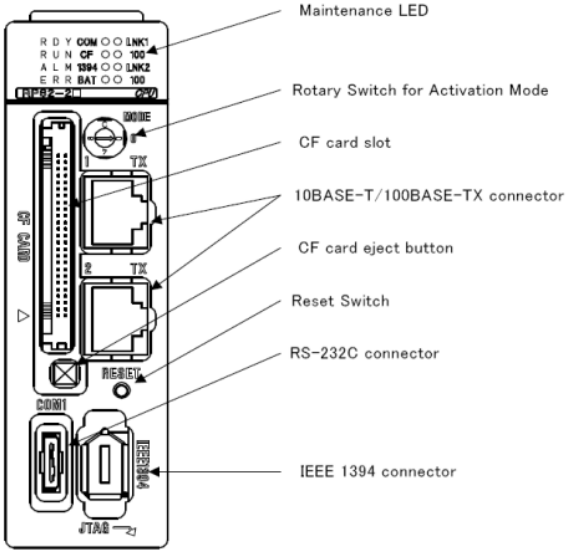

Figure 2: The Front-View of F3RP61.

THE CPU PERFORMANCE TEST

Nbench [12] benchmark is used in performance test to known RP61 CPU well. Nbench is a CPU and memory benchmark program set to test single core CPU, including NUMERIC SORT，STRING SORT，BITFIELD，FP EMULATION，FOURIER，ASSIGNMENT，IDEA，HUFFMAN，LU DECOMPOSITON test program. MEM, INT and FP Performance Index will be obtained by comparing to AMD K6-233 performance after Nbench running. MEM index is for processor bus, cache efficiency and memory performance. INT is integer computing capability of processor. FP is double float performance of CPU. All these expose the theoretical upper limit of the CPU.

The results of Nbench on RP61 are showed in figure 3. These results show that, comparing to AMD K6/233, computing intensive kind of program gain more accelerating.

Figure 4 shows the performance between RP61 and MVME5100, a widely used single border computer in physics experiment and accelerator. Nbench test shows, for CPU capability, performance of F3RP61 is closed to the MVME5100. This means that F3RP61 in compute-intensive applications have certain advantages. Comparing to traditional ladder CPU, RP61, with good operational performance, can do some more complex computing, such as advantage PID algorithm.

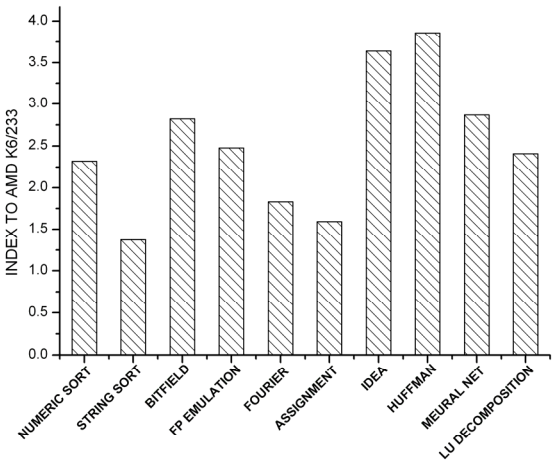

Figure 3: Ten reference program performance Index of Nbench Program Set.

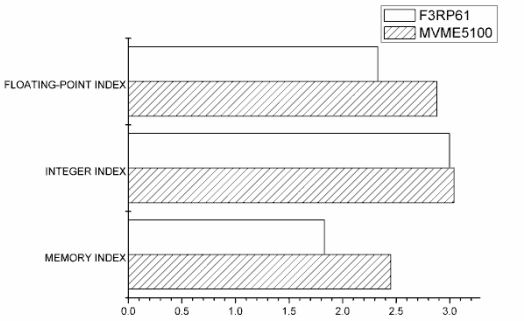

Figure 4: Performance Index Comparison. F3RP61 vs MVME5100.

NET PERFORMANCE TEST

In CSNS Experimental Control System, an important role of RP61 is information exchange node between device control layer and front control layer. So the net throughout performance and CPU utilization is an important index of performance.

Netperf [13] is a standard tool based on TCP and UDP protocol to evaluate net performance. In different test case, Netperf can do bulk data transfer or request/response test. In bulk data transfer test mode, the

result reflects how fast a system can send or receive data to/from another system.

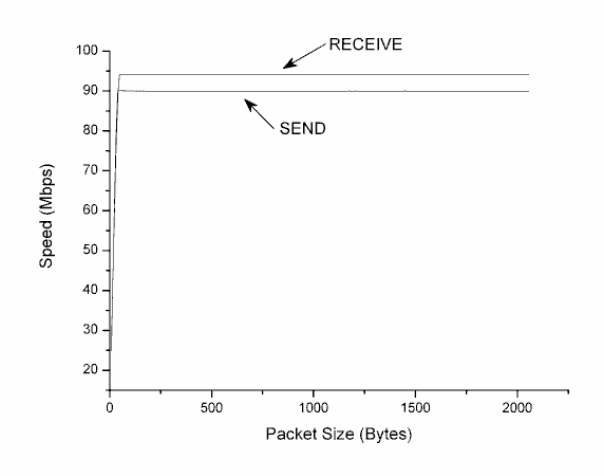

Figure 5: The net speed of F3RP61.

Figure 5 shows the send and receive speed vs. packet size of RP61 to a DELL PC. From about 100 byte, the send and receive speed can close to 100M line speed.

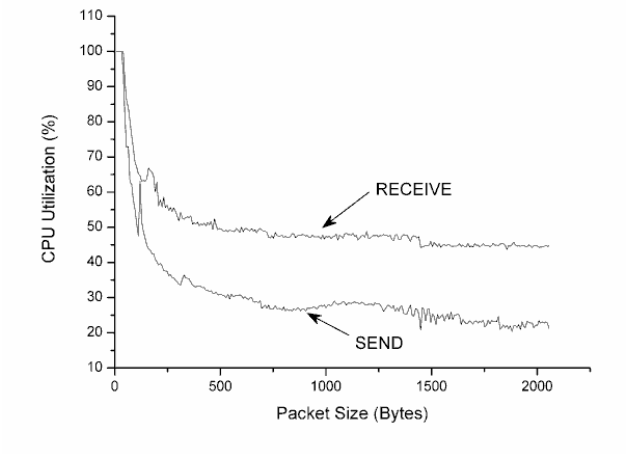

Figure 6: CPU Utilization of sending and receiving.

Figure 6 illustrate the CPU occupation with packet size. In this figure, the speed of net increases with the packet size increasing, while the CPU occupation decrease. This effect is caused by the different packing and depacking cost in TCP/IP stack in different packet size. In control system, the small size packet is dominated, so the net send task should acquire more CPU time. And also from figure 6, as more interruption happens, receive task costs more CPU time than send task. NAPI feature in the linux kernel will reduce CPU utilization obviously.

This CPU utilization of F3RP61 is much larger than MVME5100. This means, the net capability of F3RP61 is not so good.

THE PERFORMANCE ON EPICS

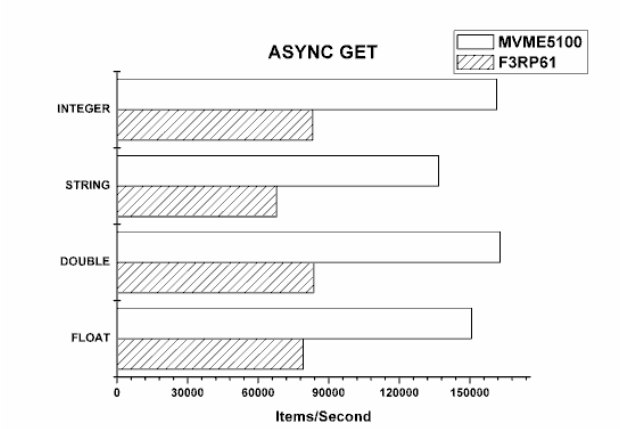

Figure 7: Asynchronous read performance comparison, MVME5100 vs. F3RP61.

In the target and instruments control system of CSNS, F3RP61 is used as information exchange node between device control layer and global control layer, providing PV service and control information exchanging. Besides this, F3RP61 can provide some control functions within epics framework. So how to evaluate and balance these two functions is the problem in front of target and instruments control system.

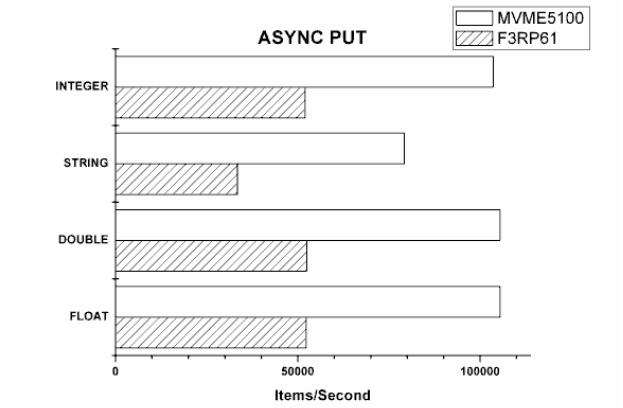

Figure 8: Asynchronous Write performance comparison, MVME5100 vs. F3RP61.

The main tasks of EPICS are providing periodic scan for control and PV access from Ethernet. We can estimate the maximum PV access the F3RP61 can provide through the test to provide design roof for the system design.

EPICS IOC performance on F3RP61 can be estimated through PV access speed test. Figure 7, 8, 9 shows F3RP61 PV access speed comparing to MVME5100. In this test, F3RP61 and Dell PC are connected in the same CISCO 3750 switch. F3RP61 can provide about one half PV access of MVME5100 in case of full CPU occupation. Considering real-time information exchange and reliable PV access service, 20% CPU time can be used to PV

service on information exchange dominant node. More less CPU time, about 5% to 10%, can be allocate to PV access in hybrid node of information exchange and control.

Synchronous read speed is much slower than asynchronous access speed. The reason much time is cost in waiting the response on net.

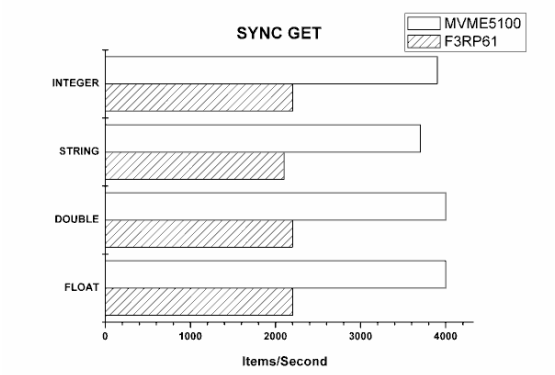

Figure 9: Synchronous read performance comparison, MVME5100 vs. F3RP61.

For control task, the stability of scan period is most important. Figure 10 depicts the output of IOC period scan on F3RP61. The scan period in this chart is 5ms. The period of output is 10ms. The default EPICS configuration was used. After more than 190,000 samples, the Std. Dev. of scan period is about 26us. The Max-min jitter is about 600us. For the general control task, the typical period is about tens of millisecond. This deviation can be accepted.

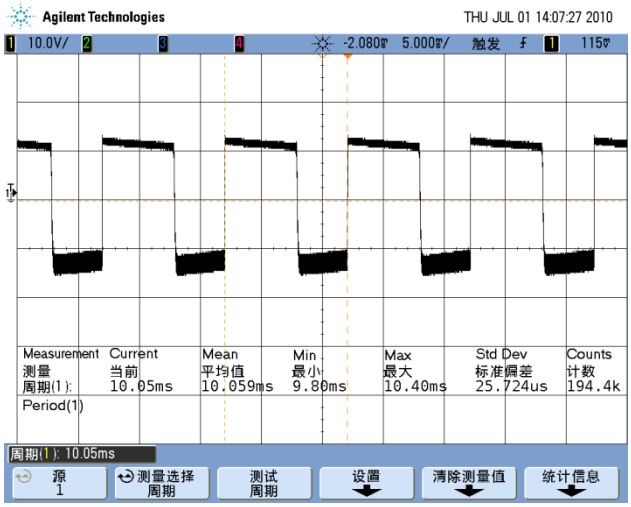

Figure 10: Jitter of 10ms period.

CONCLUSION

Through all the tests in this paper, the conclusion that F3RP61 can be used as information exchange and control node in the target and instruments control system of CSNS can be drawn. Comparing to traditional ladder CPU, F3RP61 is able to do more computing，to run EPICS and to provide more information exchanging.

REFERENCES

[1] A. Uchiyama et al. “Development of Embedded EPICS on F3RP61-2L”, Proc of PCaPAC2008, Ljubljana, Slovenia, Oct. 2008, pp.145-147

[2] S. Araki et. al., “Magnet Power Supply Control Based on EPICS on F3RP61 for KEK-ATF”, Proc of ICALEPCS2009, Kobe, Japan, Oct. 2009,

[3] S. Motohashi et. al., “Data Acquisition System of Beam Loss Monitors of J-PARC Main Ring”, Proc of ICALEPCS2009, Kobe, Japan, Oct. 2009,

[4] M. Komiyama et al., “Upgrading the Control System of RIKEN RI Beam Factory for New Injector”, Proc of ICALEPCS2009, Kobe, Japan, Oct. 2009, pp.277-279

[5] M. Takagi et al., “Control of the J-PARC Slow Extraction Line Based on Embedded EPICS”, Proc of ICALEPCS2009, Kobe, Japan, Oct. 2009, pp.549-551

[6] T. Nakamura et al., “Upgrading the Control System of the Movable Masks for KEKB”, Proc of ICALEPCS2009, Kobe, Japan, Oct. 2009, pp.546-548,

[7] K. Mikawa et al., “Embedded EPICS Controller for KEKB Pulsed Quadrupole Magnet Power Supply”, Proc of ICALEPCS2009, Kobe, Japan, Oct. 2009, pp.558-560,

[8] J. Odagiri et al., “Application of EPICS on F3RP61 to Accelerator Control”, Proc of ICALEPCS2009, Kobe, Japan, Oct. 2009, pp.916-918,

[9] C.Y. Wu et al., “Control of the Pulse Magnet Power Supply by EPICS IOC Embedded PLC”, Proc of IPAC2010, Kyoto, Japan, May. 2010, pp.2731-2733

[10] T. Kosuge and K. Nigorikawa, “STARS on PLC, Proc of PCaPAC2010”, Saskatoon, Canada, Oct. 2010 pp.73-75.

[11] J. Odagiri et al., “Development of Image Processing System on Embedded EPICS for Beam Diagnostics”, Proc of PCaPAC2010, Saskatoon, Canada, Oct. 2010, pp.165-167

[12] http://www.tux.org/~mayer/linux/bmark.html

[13] http://www.netperf.org/netperf/

[14] RTOS-CPU module (F3RP61) Linux BSP Reference Manual, Yokogawa, Japan

[15] RTOS-CPU Module (F3RP61) Hardware Instruction Manual, Yokogawa, Japan