

SuperB Linac VME Beam Position Monitor

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Acknowledgements

- Thank you for your hospitality!
 - It has been a great pleasure to visit KEK and work with all of you.
 - Kazuro Furukawa, Ryo Ichimiya, Tsuyoshi Suwada, other people
 - Looking forward to continued collaboration!
- Developments
 - Congratulations on taking on an ambitious project!
 - Much work has been completed
 - It was a GREAT to work on your board and make modification to a working board!

Charge

- Review linac beam position monitor VME hardware
- Suggest:
 - possible improvements
 - how to evaluate performance
 - Path forward

Overview

Scope

- ~100 stripline BPMs in linac

- Requirements
 - Beam charge range: 0.1 to 5nC (10 nC?)
 - Resolution σ_{xy} < 10 microns at 1 nC
 - <100 microns at 0.1 nC</p>
 - Scale: 10 micron resolution requires measurement to ~0.2%
 - Two bunches at 96 ns separation
- Schedule
 - Demonstrate performance by fall 2013
 - Order production units January 2014
 - Start commissioning Oct 2014

Overall Recommendations

- Evaluate:
 - Noise
 - Effective number of bits (ENOB)
 - Front-end noise
 - Linearity
 - Third-order intercept (IP₃)
 - · Set attenuators to optimize noise vs. linearity
 - Understand signal level at every potentially non-linear stage
 - Important for
 - stability with clock phase variation
 - Stability with beam current variation
- Study:
 - Position algorithm
 - Calibration Scheme (SLAC calibrates Red and Green, KEK Calibrates Red,Green,Yellow, Blue) but KEK has beam come between Green and Yellow. Is this needed or does this add offsets from shot to shot?
 - 2-bunch algorithm
 - Document procedures

Overall Recommendations (2)

- Because this is a very ambitious project, KEK needs additional staff to:
 - Perform studies,
 - Develop algorithm
 - RF designer to look at front-end and filter responses
 - FPGA person to make sure FIFO is behaving properly
 - Grad student or post-doc?
 - maybe 2 additional people
- KEK needs synchronous acquisition of BPMs, other pulse-pulse diagnostics (What is the timing system?)
 - Very difficult to understand jitter, drift, optics without synchronous acquisition
 - Linac is a different machine every pulse when you look at high resolution

Evaluate ADC Noise

- Does ADC deliver expected performance?
 - What is the VME ADC noise level without an input signal matches ADC spec
 - Evaluate the VME ADC with a signal present
 - Understand Clock Jitter and how it effects ENOB
 - Understand filter responses and what the VME ADC will see (Nyquist folding)
 - Understand RF input bandwidth, ADC input Bandwidth

Evaluate Linearity

- Linearity crucial for stability against
 - Clock phase
 - Beam charge variation
- Assume linearity well-characterized by third-order inter-modulation performance
- Measure Third-order intercept (IP₃)
- Inject 2 tones (F₁ & F₂) separated by a MHz through combiner
- Each tone at Full scale -7dB (so sum doesn't saturate)
- Evaluate spectral components at 2*F₁-F₂ and 2*F₂-F₁
 - Either by digitizing with ADC and FFTing ADC counts
 - Or use spectrum analyzer on analog signal and calculate IP3
 - Do both steps to understand the spectral contents of each circuit

VME Recommendations

- Understand why resolution isn't as expected
 - What is the ADC input network and how it is affected by ADC sampling spikes, and what is the input bandwidth?
 - Is the ADC noise low enough?
 - Is the ADC linearity good enough?
 - Filter response
 - Tails extending across Nyquist zone boundaries?
 - 2nd passband in filter response at 900 MHz? (Need to reduce/eliminate this spectral content.)
- Verify ADC performance
 - Noise (ENOB)
 - Linearity (IP₃)
- Verify First Stage(Front-end) Amp(s) / Bandpass Filter performance
 - Noise (nV/sqrt(Hz) or dBm/Hz)
 - with spectrum analyzer, or through ADC
 - Linearity (IP₃)

VME Recommendations (2)

- Change ADC input bandwidth to achieve 300 MHz
 - We provided a solution for this and will discuss this later in the talk
- Improve filter response
 - Keep tails of filter response between -40 to -50 dB at Nyquist zone edges
 - (if possible using factory made filters Lark, K&L, Lorch, TTE, Japan company)
 - Remove/reduce 2nd passband near 900 MHz
- Improve ADC input network
 - Maintain response to 300 MHz then roll off
 - Follow SLAC input circuit or Analog devices suggestion
- Understand algorithm
 - How many samples should be included? (i.e. digital windowing)
 - How should attenuators be set to optimize noise vs. non-linearity?
 - Keep signal levels $< IP_3 30 \text{ dB}$ (3rd order products < -60 dB)
 - (SLAC can help with Simulink simulations and excel spreadsheet)

VME Recommendations (3)

- Possibly improve First Stage Amplifier(s) noise figure
 - This is low priority, not very important
 - Already better than needed for required resolution
- Calibration switch scheme to improve isolation and offsets
- Input delay circuit
 - Is it needed and what does it do to the freq response of the RF front-end? SLAC matches cable lengths instead and designs the PCB to have matched group delay within 1ns.

Measuring Two Bunches

- Two-bunch performance is important for identifying and correcting wakefield kicks
- Measurement of two bunches not yet demonstrated
- Recommendations:
 - Beam test
 - Create artificial 2nd bunch with splitter, delay, combiner
 - Expect to measure same position of two bunches
 - Offline synthetic 2nd bunch
 - Record waveforms from single bunch beam
 - Add signal from opposite strip, delayed by 96 ns
 - Expect 2nd bunch position opposite of 1st.
- Test with 2 bunch beam as soon as possible

KEK VME BPM Module

Two boards make this module

Analogue Frontend (sub board)





(G) 2PULSE BPM 40 OVER (0) D 0 NG NG . 0 ö 200 Ø 18K12 DIGITEX

KEK Noise problem

AD converted data (readout)

• 300MHz tone pulse are sampled at 250MS/s (under-sampling method).



- Almost same height and single AD clock cycle pulses (noise) are observed.
 - •On an adjacent channels, same phenomenon is observed too.
 - Bit pattern:

•Normal data: 1000_0000_0000_XXXX •Noise data: 1000_0101_0101_XXXX

Such a kind of noises may happen at FIFO input and/or ADC inside. (decimation?)

KEK Schematic modifications

- Finally we find two remedies to remove this noise.
 - 1. Insert 22pF capacitor between differential signal line at ADC input.
 - Act as LPF and normal-mode noise stabilizer.
 - 2. Tune Data/Clock timing at FIFO by 0.2ns (tentative).
- Both remedies are mandatory to fix this problem. So, we guess both causes contribute. (inside ADC malfunction, metastable at FIFO input)



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Response of KEK filter

circuit parameter changes



The 22pF limited the BW to the ADC, this is why Steve Smith suggested going to a lower frequency front end.

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SLAC Schematic Quick Modifications

Using 1mm by 0.5mm resistors I modified The VME board to place the 20ohm resistors and the 1.8pF cap in a place where there were only two pads for the 15 ohm resistor (i,.e., creating a resistor totem pole).



Time-Domain Response



A factor of ~10dB improvement in SNR. Did not improve the resolution, why?? Did not have enough time to figure out why there was no improvement. Would like understand why that happen.

Further ADC Improvements



SLAC Circuit uses Coilcraft transformers and RF front end electronics. SLAC has designed anti-aliasing filter at the input of ADC.

Recommendation

- Many areas to look at for improvement; Front-end Bandwidth, noise, clock jitter, calibration scheme
- VME <u>should</u> get much better than 10 micron resolution at 1 nC
 - Presently limited by ADC input network, possibly excess noise
 - SLAC gets 4micron at 250pC. Need to determine what are the difference between SLAC and KEK and make changes.
- Calibration is very important
 - VME can calibrate frequently (or continuously)
 - Verify Calibration Scheme
 - Make sure calibration switches provide good isolation
- SuperB VME solution is a very good solution keep pursuing it!
- Work with SLAC to make this a State-of-Art BPM and consistent with SLAC uTCA development.

Thank you